

COMPAL CONFIDENTIAL

MODEL NAME :  
FDI40 N3-14", FDI4A V3-14", FDI43 N5-14",  
FDI50 N3-15", FDI5A V3-15", FDI53 N5-15",  
FDI70 N3-17"

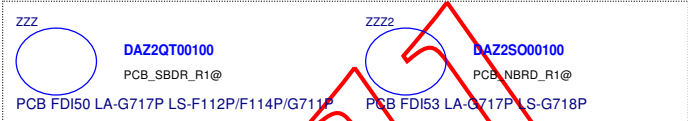
PCB NO : DA60027S000 (SBDR)  
DA60027S100 (NBDR)

BOM P/N :

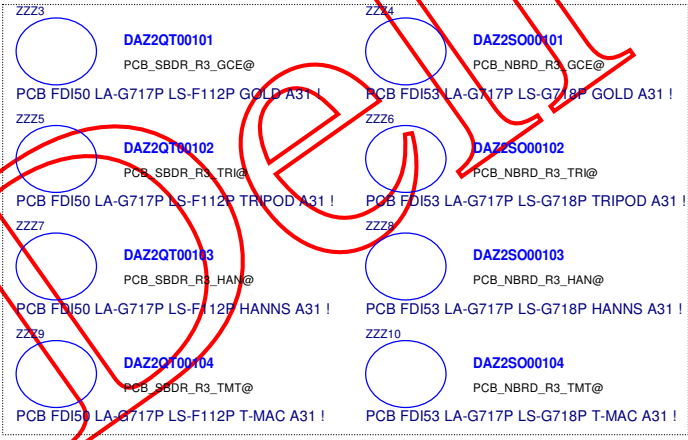
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431AJ331L51 431AJ331L54	431AJ331L01	X4E AJ331L51(N3)
431AJ331L52 431AJ331L55	431AJ331L02	X4E AJ331L52(V3)
431AJ331L53 431AJ331L56	431AJ331L03	X4E AJ331L01(N5)

CML-U+MEC1418  
2019-06-19  
REV : 1.0 (A00)

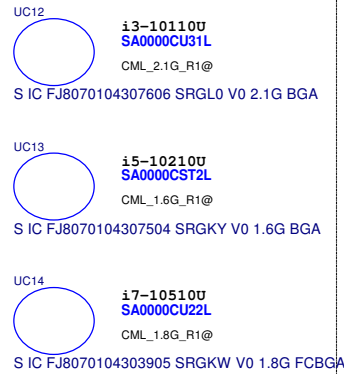
PCB R1



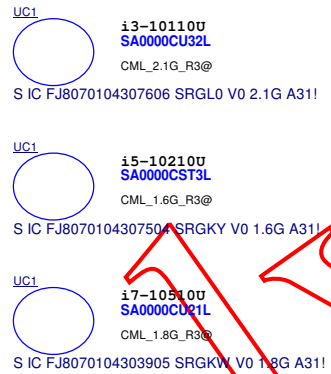
PCB R3



CPU R1



CPU R3



@ : Un-pop Component  
DIS@ : GPU Support  
N3@/V3@ : Inspiron/Vostro  
CML@/CNL@ : CML/CNL  
BASE@/PREM@ : (Pentium)(Celeron)i3 i5 i7

EC@ : EC Support  
JP@/PJP@ : JUMP  
100@/1000@ : Lan

EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
CMC@ : XDP Component  
CONN@ : Connector Component  
KBL@ : KB Backlight  
TPM@/FTPM@ : HW TPM/SW TPM  
750 CTPM@:750 and china TPM  
ST CTPM@:ST and china TPM  
CTPM@:China TPM  
FFS@ : Free Fall Sensor  
TYPEC@ : TypeC  
TYPEC@EMI@/TYPEC@ESD@: EMI, ESD ,TypeC Component

PCB@/PCB\_R1@/PCB\_R3\_G@/PCB\_R3\_T@/PCB\_R3\_H@/PCB\_R3\_TM@: PCB MB

PCB\_NBRD\_R1@: PCB MB for NBDR  
TS\_NON@/TS\_USB@/TS\_I2C@: Touch Screen Interface Select  
SBDR@/NBDR@: SBDR/ NBDR Select

Layout Dell logo

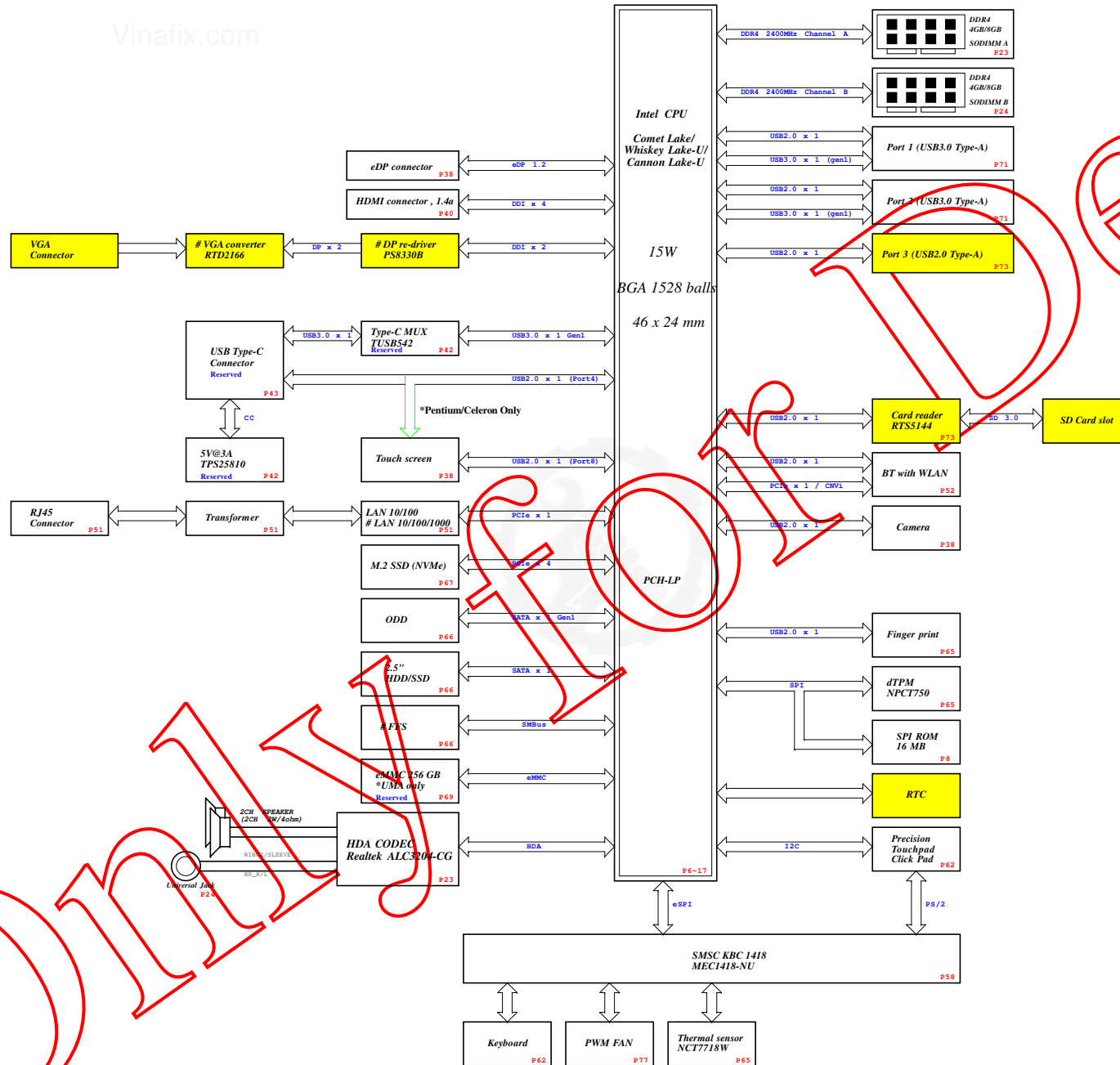
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REV: X00  
PWB: 9HTP8

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Size	Document Number	Rev		LA-G717P	
Date:	Wednesday, June 19, 2019	Sheet	1 of 100		

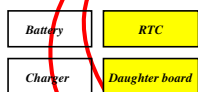


# Block Diagram

Vinafix.com



# ----> Laptop only





## POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

## Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A
+RTC_CELL	RTC power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 Port, IO/B
4*	Touch screen
5	Finger printer
6	Camera
7	Card reader , IO/B
8*	Reserved
9	NA
10	BT

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 port1
USB3.0-2	PCIE-2		NA
USB3.0-3	PCIE-3		USB3.0 port2
USB3.0-4	PCIE-4		TypeC
USB3.0-5	PCIE-5		
USB3.0-6	PCIE-6		
	PCIE-7		
	PCIE-8		
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1A	SATA ODD
	PCIE-13		NVME SSD
	PCIE-14		NVME SSD
	PCIE-15	SATA-1B	NVME SSD
	PCIE-16	SATA-2	NVME SSD

## Board ID & Model ID Table

#	Pull-down	Pull-up	Voltage	Board ID	Model ID
1	100	10.0	3.000	EVT	SBDR-UMA
2	100	17.8	2.801	DVT1	
3	100	27.0	2.598		NBDR-UMA
4	100	37.4	2.402	DVT2	
5	100	49.9	2.201		SBDR-DSC
6	100	64.9	2.001	Pilot	
7	100	82.5	1.808		NBDR-DSC
8	100	107.0	1.594		
9	100	154.0	1.299		
10	100	200.0	1.100		

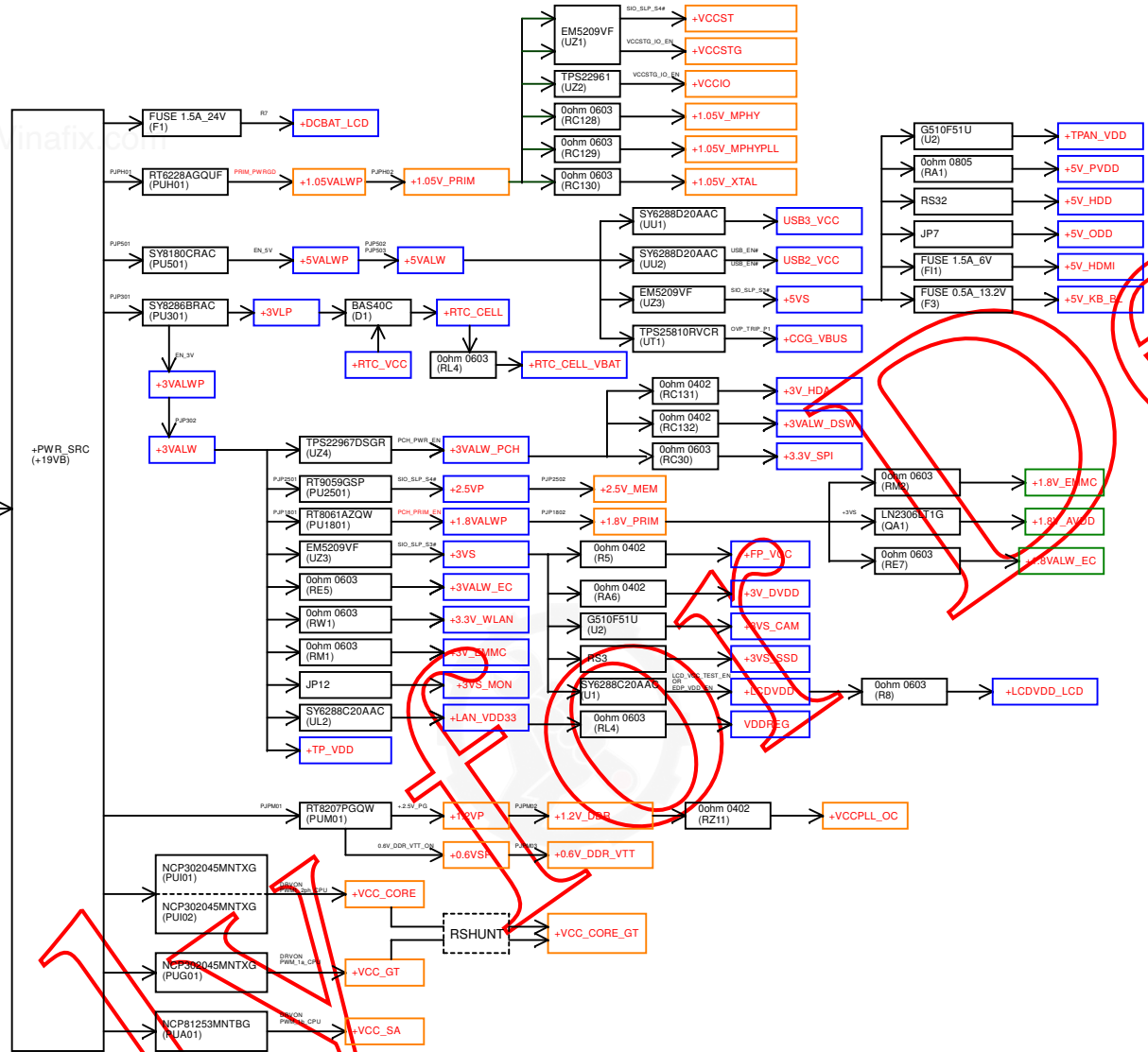
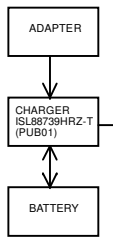
Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support					No Support					Yes				Yes	

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				LA-G717P	Rev 1.0
				Date: Wednesday, June 18, 2019	Sheet 3 of 100



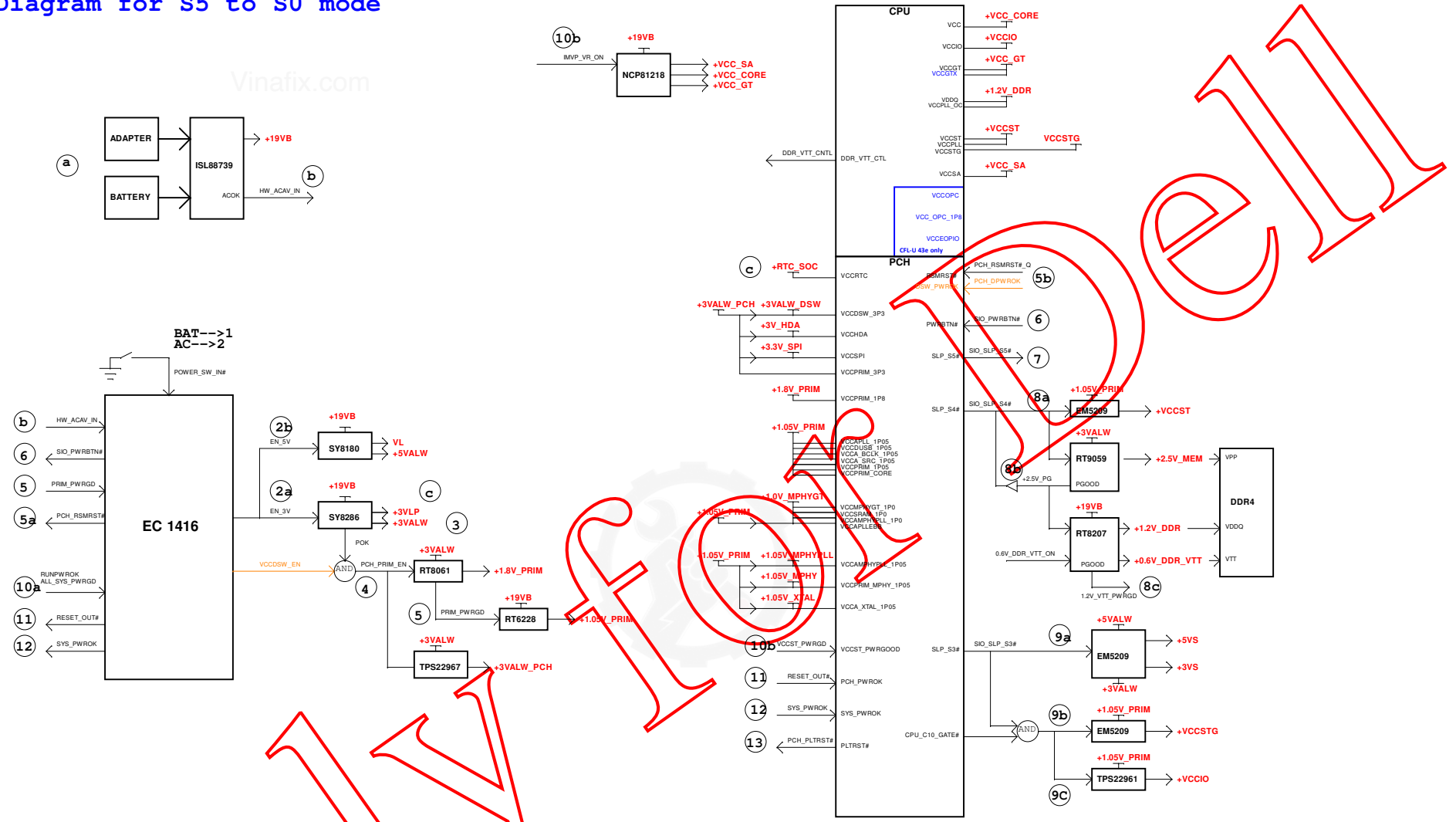
CPU PWR  
GPU PWR  
Peripheral Device PWR



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			LA-6717P	
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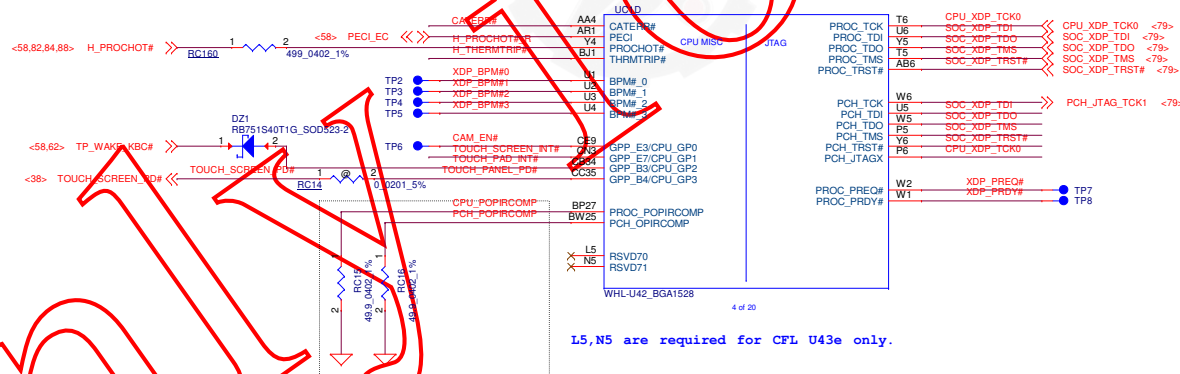
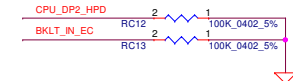
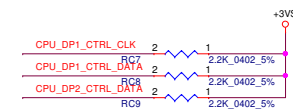
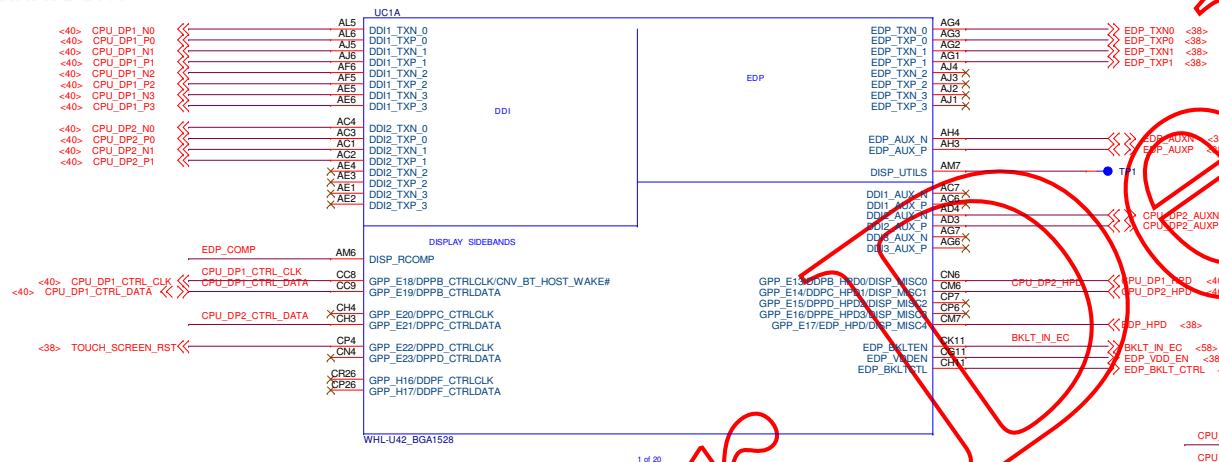
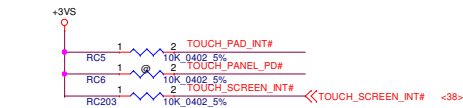
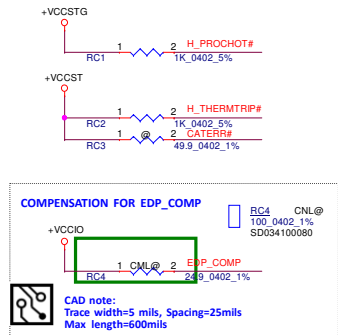
Timing Diagram for S5 to S0 mode



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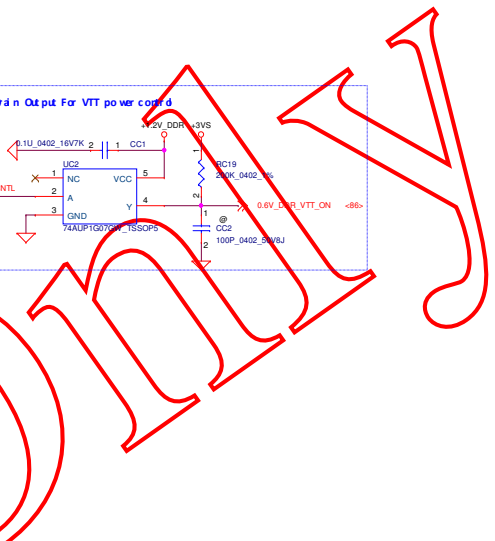
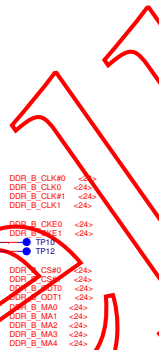


**COMPENSATION FOR OPORCOMP**

CAD Note:  
Min trace width=10 mils, Max trace length=500 mils

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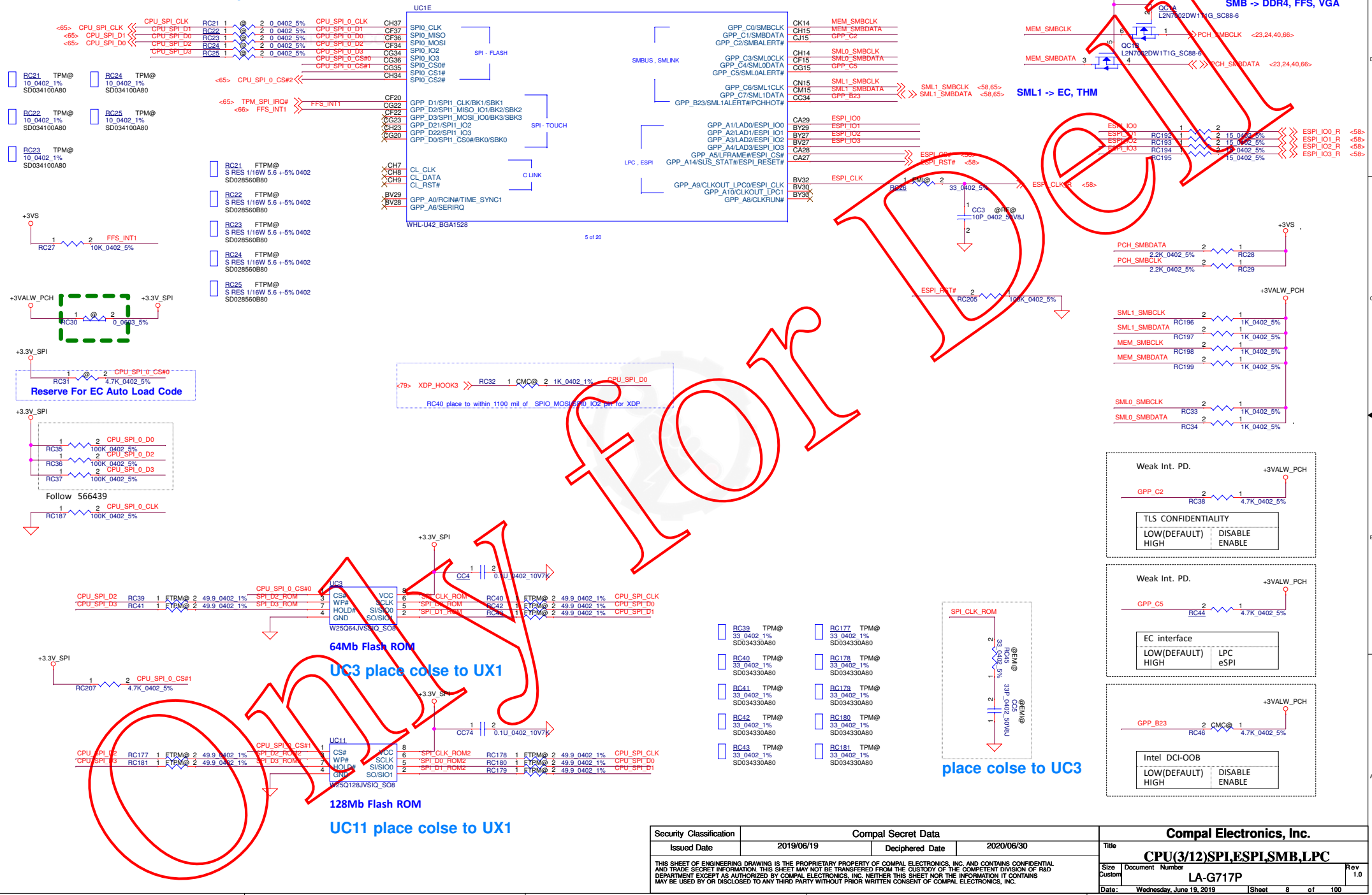




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				Rev		
				1.0		
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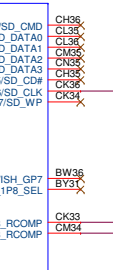
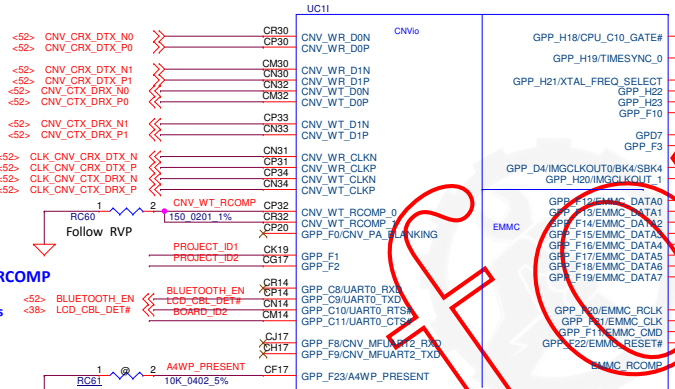
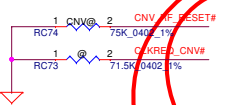
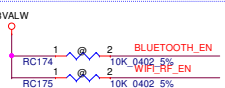
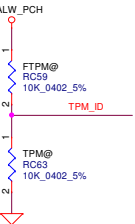
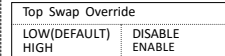
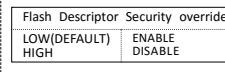
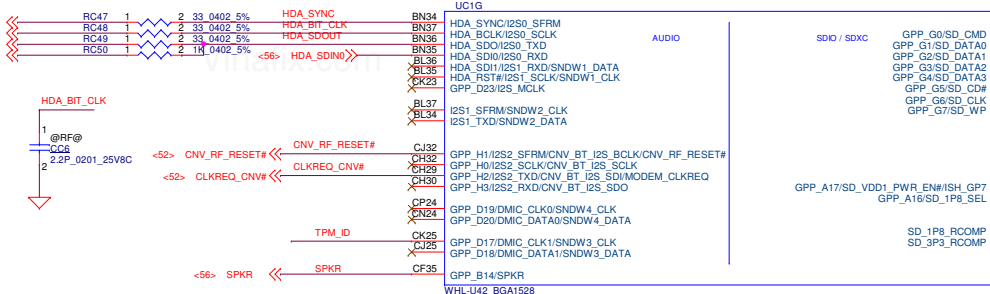
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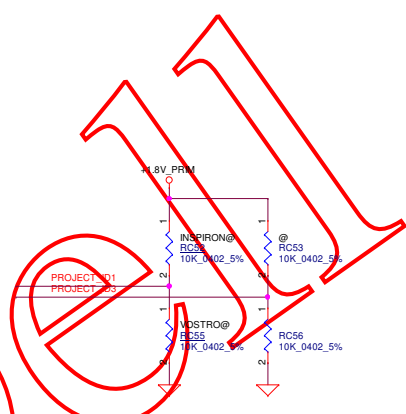
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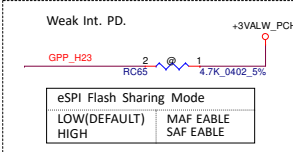
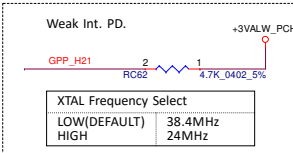
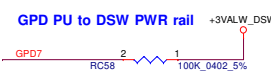
LOW = ENABLE -->ME lock, can't update ME  
HIGH = DISABLE -->ME un-lock, can update ME



 **COMPENSATION FOR SD\_RCOMP**  
CAD Note:  
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Max trace length=500 mils



RC53,RC56	
eMMC SKU Option	
LOW	Standard
HIGH	Narrow Border



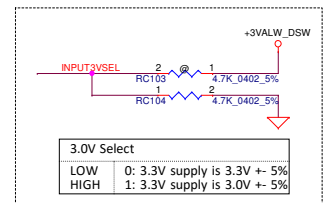
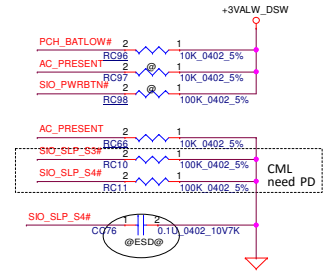
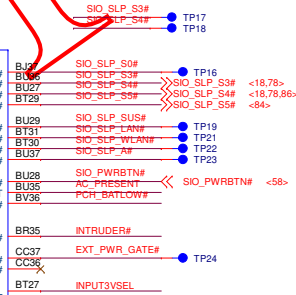
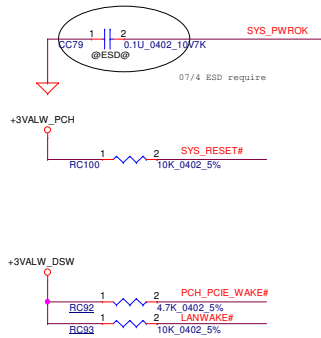
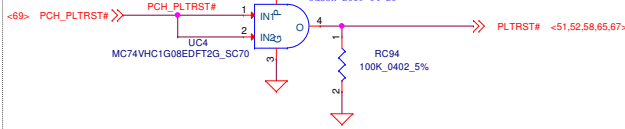
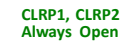
CPU ID	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
CML-U	---	RC70
WHL-U(Reserved)	---	RC72
Pentium/Celeron	RC69	---
i3/i5/i7	RC71	---

PROJECT_ID2	
LOW(DEFAULT)	UMA
HIGH	DIS

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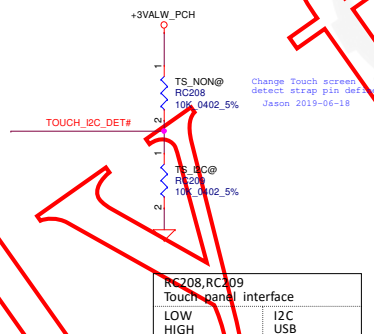
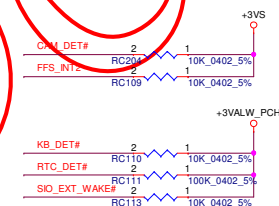
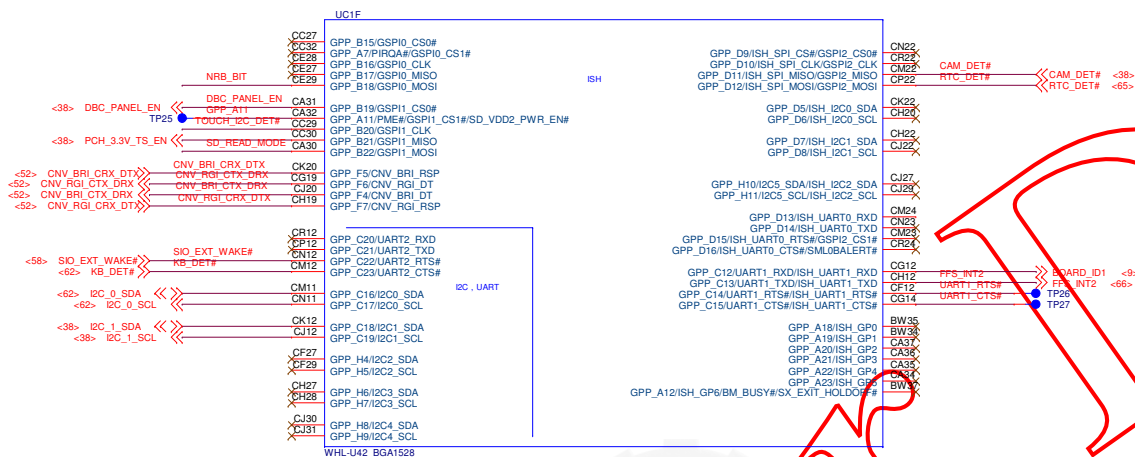
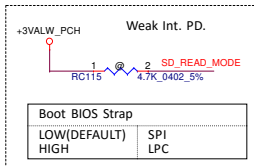
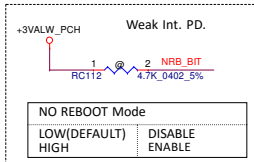
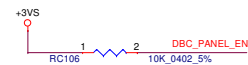


WLAN-->



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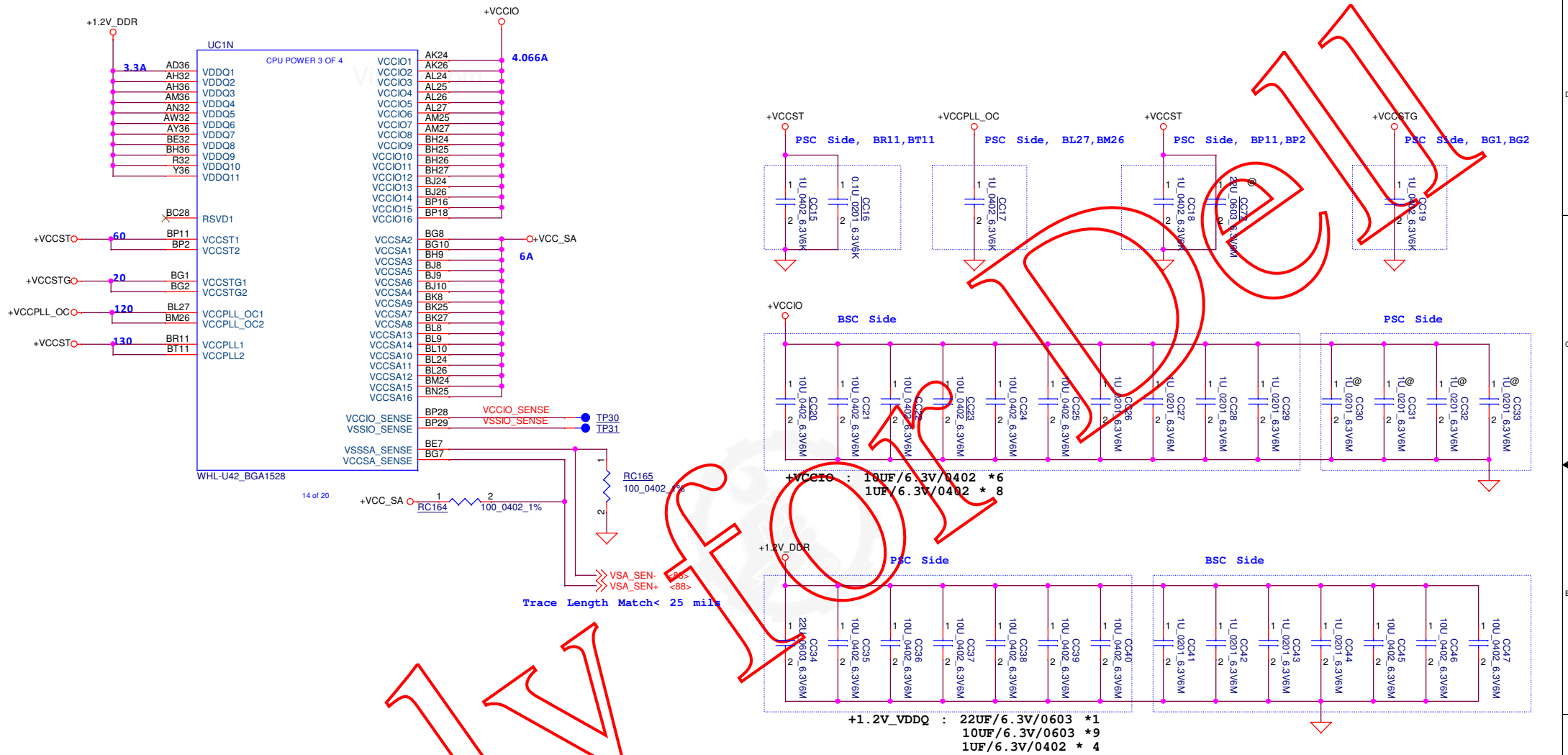
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						Date:		Wednesday, June 19, 2019		Sheet 11 of 100	



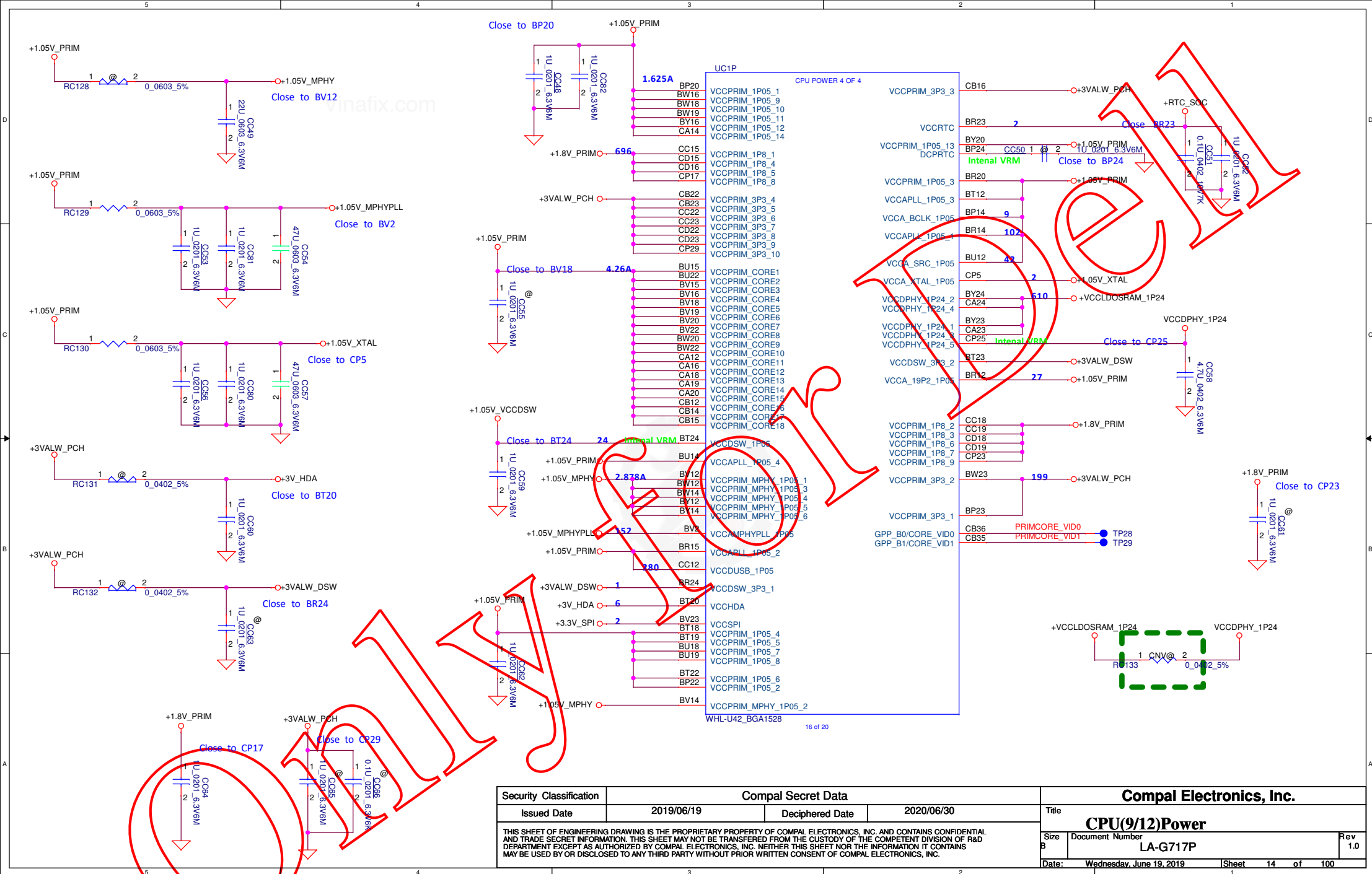




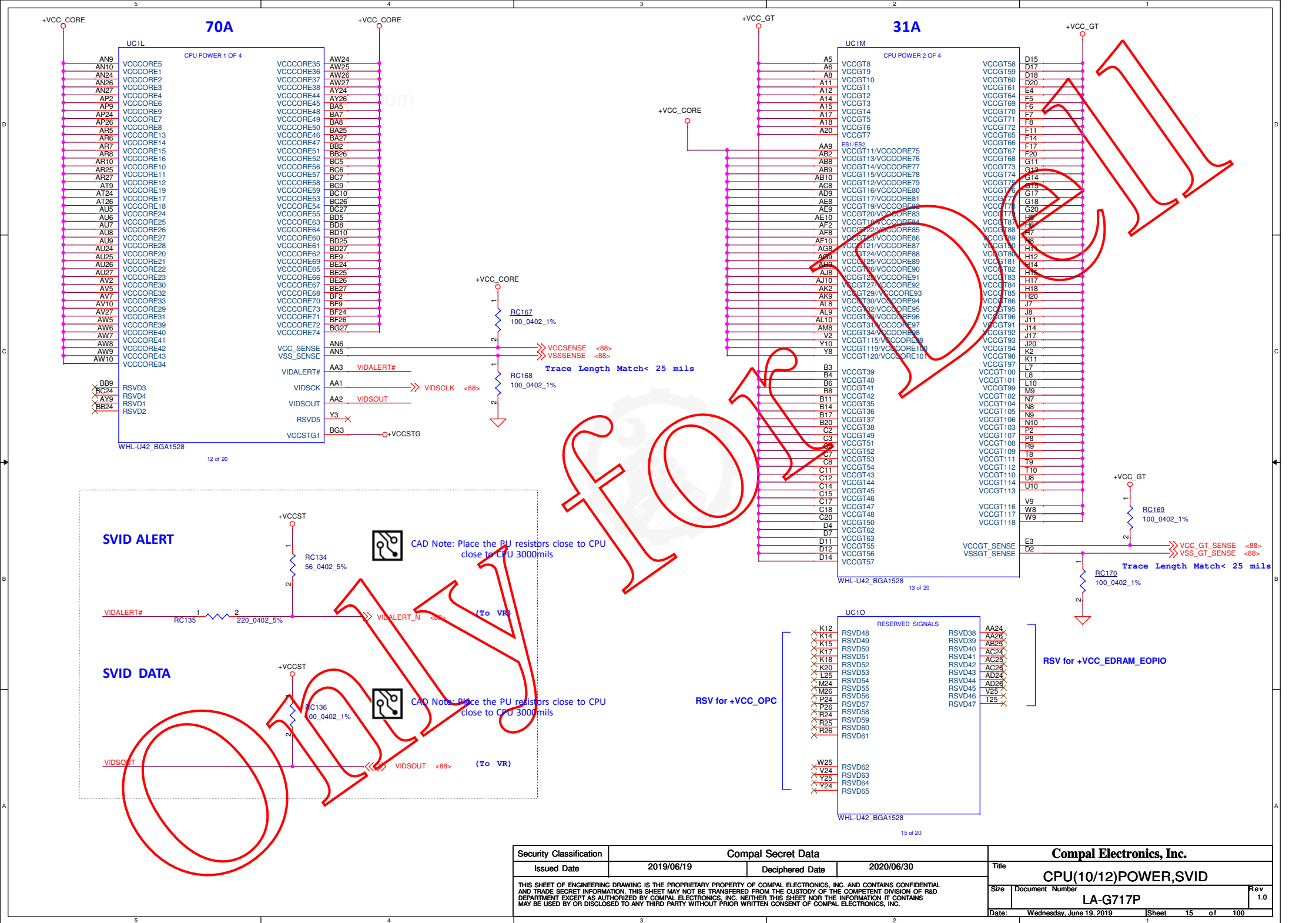


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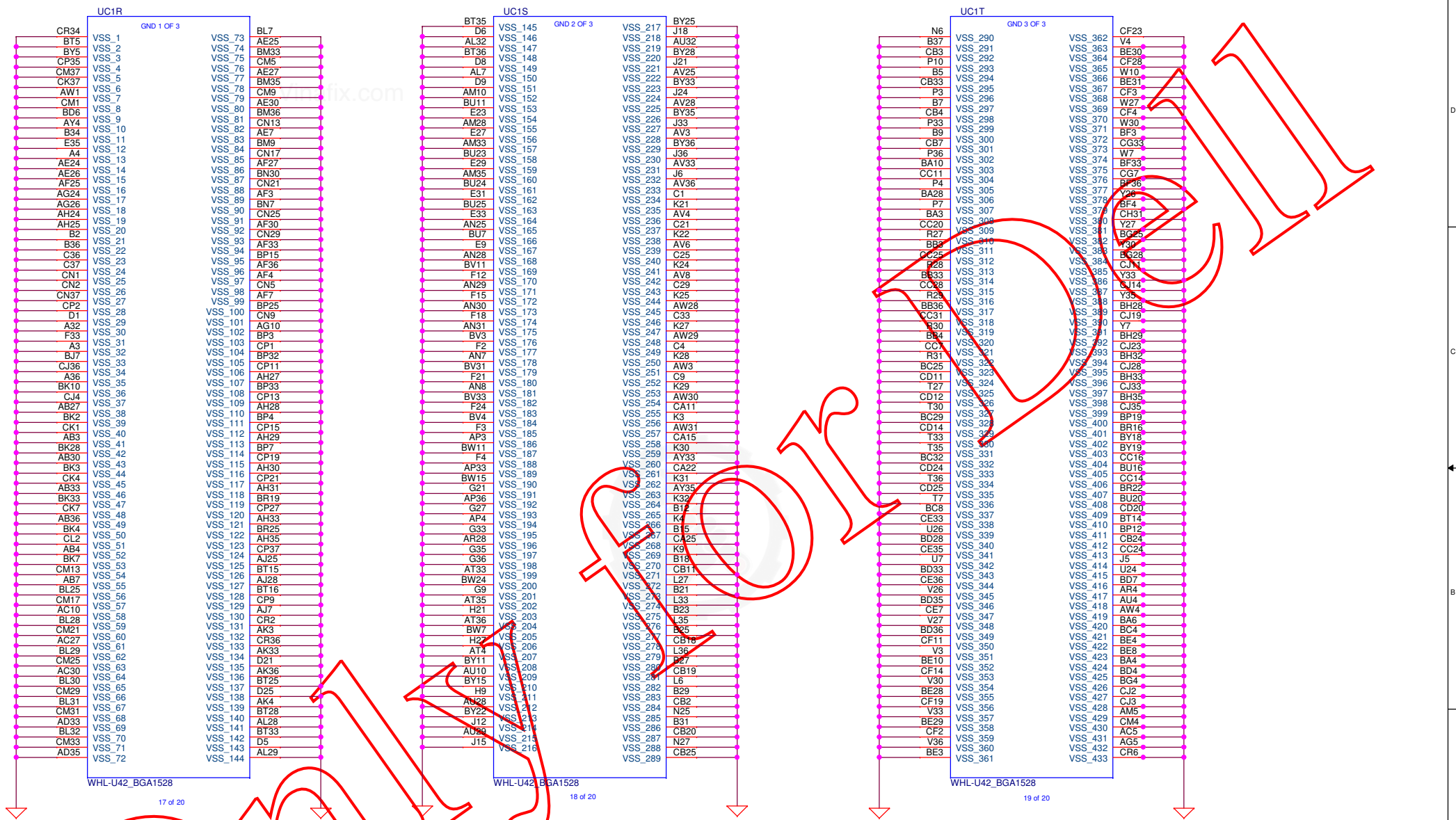








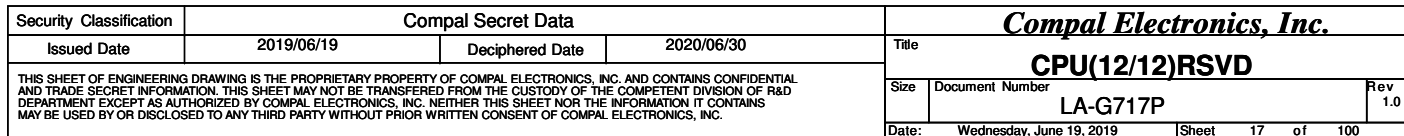




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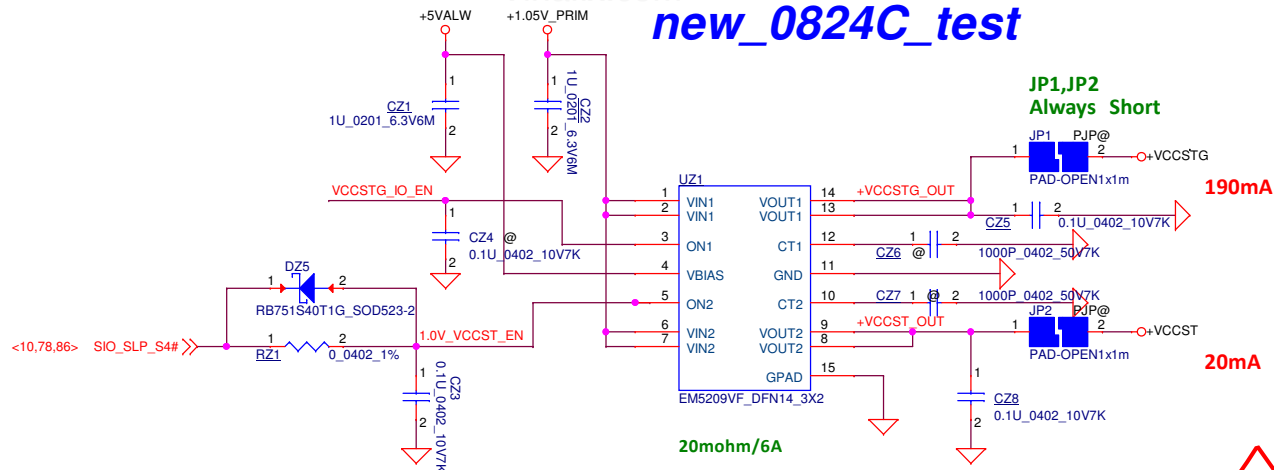
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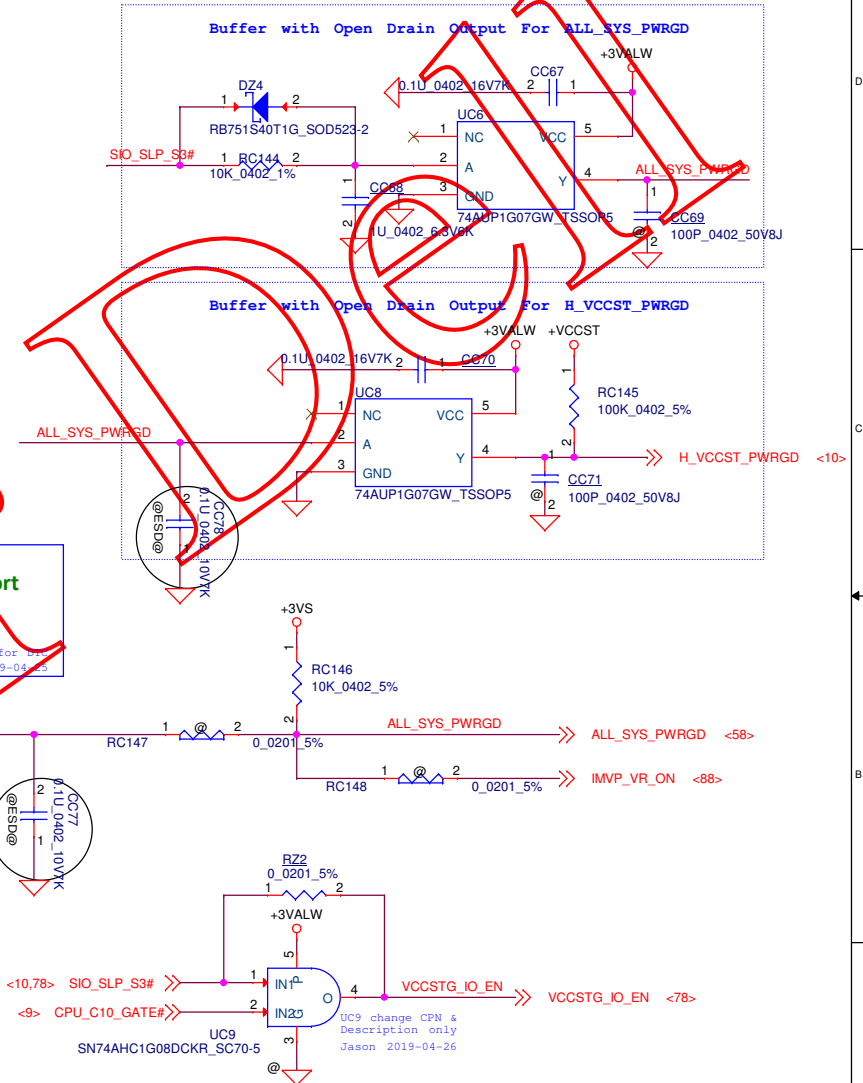
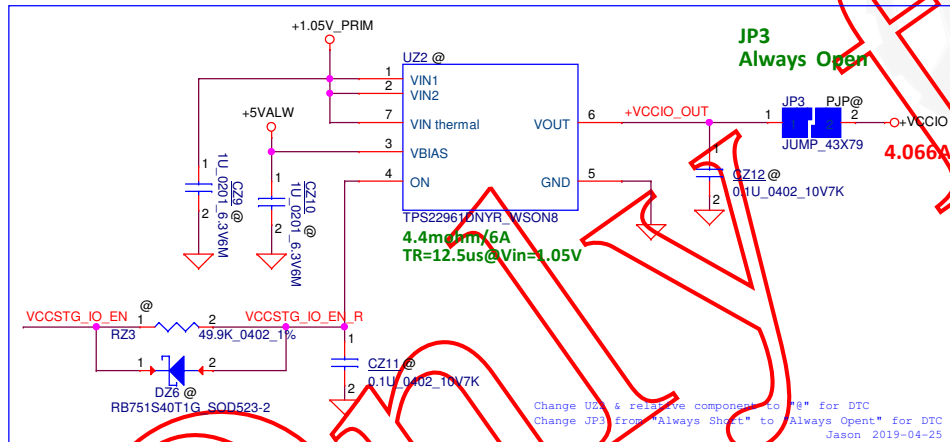


**+1.05V\_PRIM TO +VCCST /+VCCSTG**

**new\_0824C\_test**



**+1.05V\_PRIM TO +VCCIO**



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										CPU PWR GATE	
										LA-G717P	
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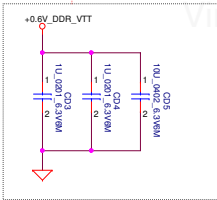
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				Document Number	1.0
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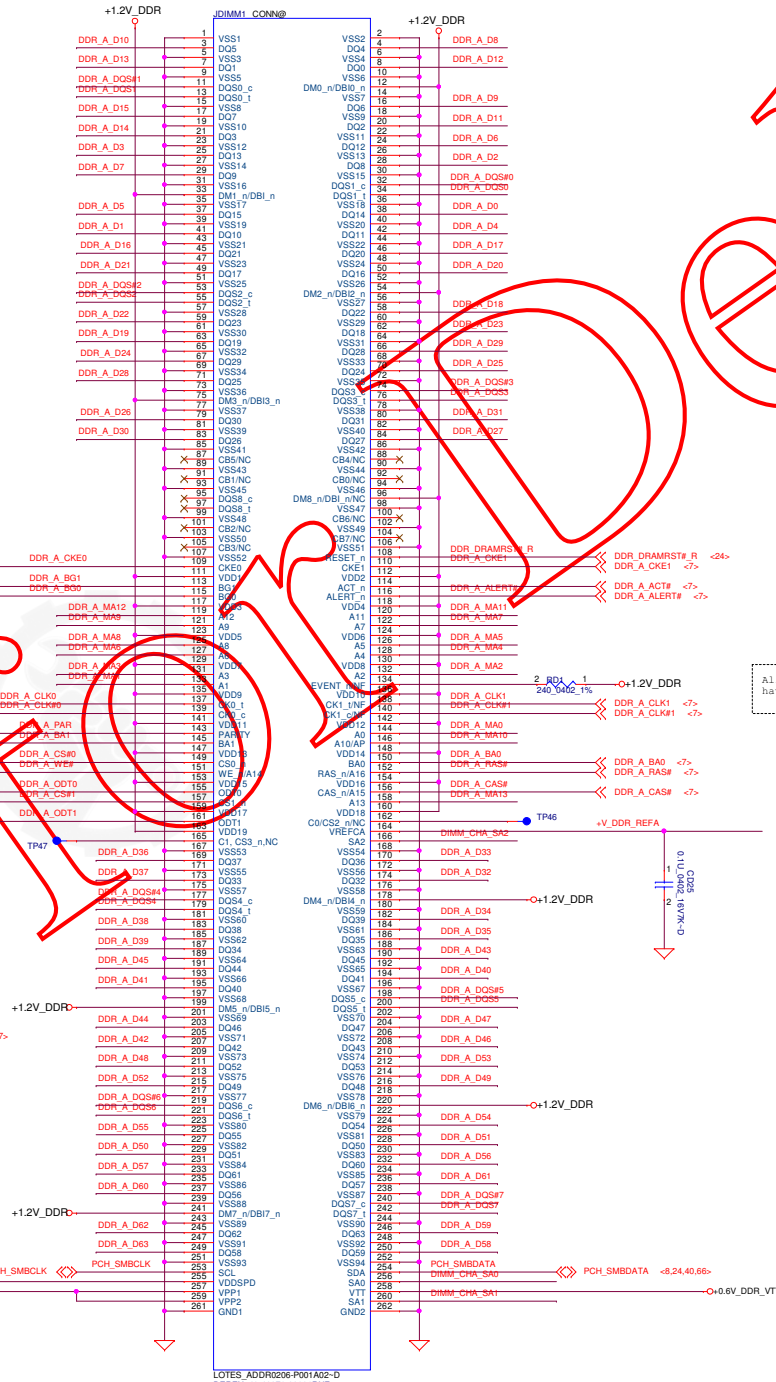
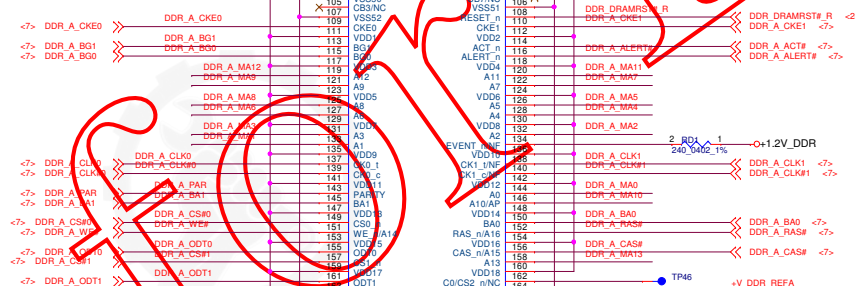
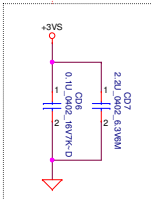


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<7> DDR_A_MA[0..13]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_DQS[0..7]
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Layout Note:  
Place near JDIMM1.258



Layout Note:  
Place near JDIMM1.25



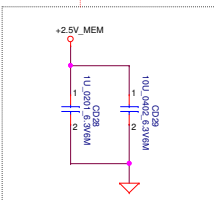
All VREF traces should have 10 mil trace width

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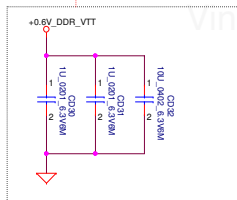


Main Func = DDR

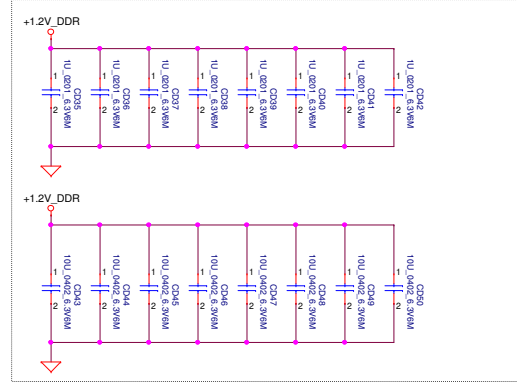
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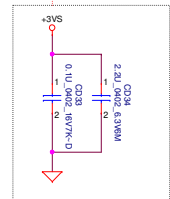
Layout Note:  
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Layout Note:  
Place near JDIMM2



Layout Note:  
Place near JDIMM2.255



<7> DDR\_B\_D0[83]  
<7> DDR\_B\_MA0[13]  
<7> DDR\_B\_DQS[0..7]  
<7> DDR\_B\_DQS[0..7]



All VREF traces should  
have 10 mil trace width

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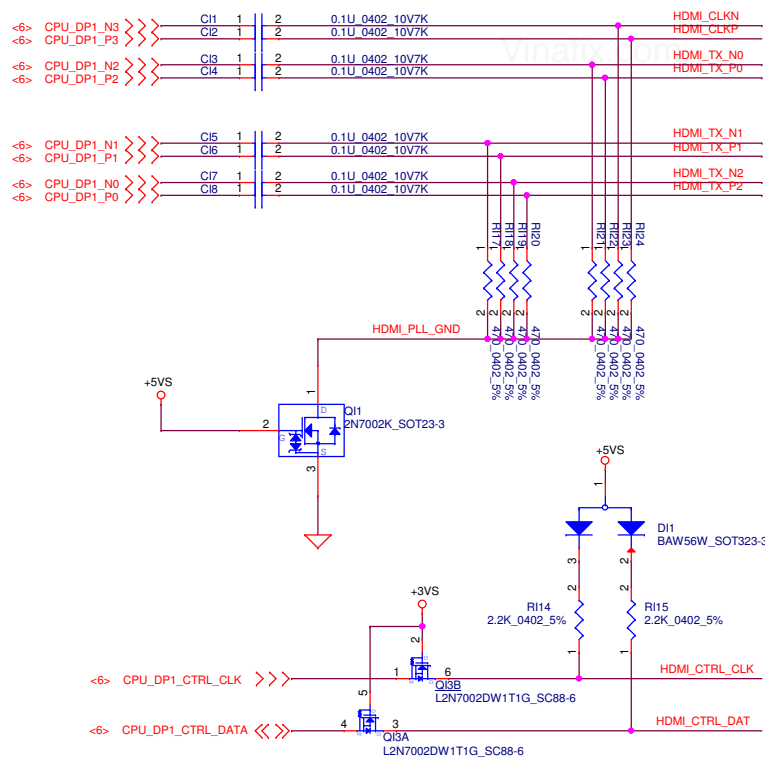
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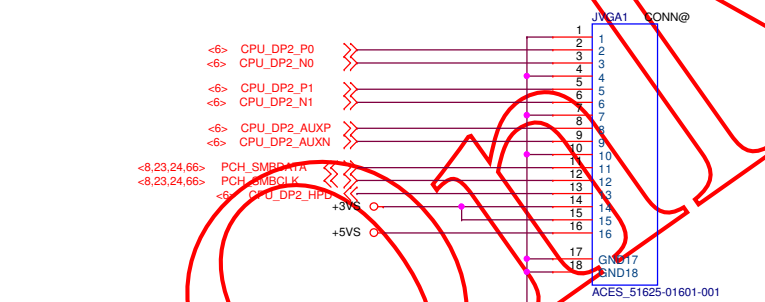
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Main Func = HDMI



Main Func = VGA





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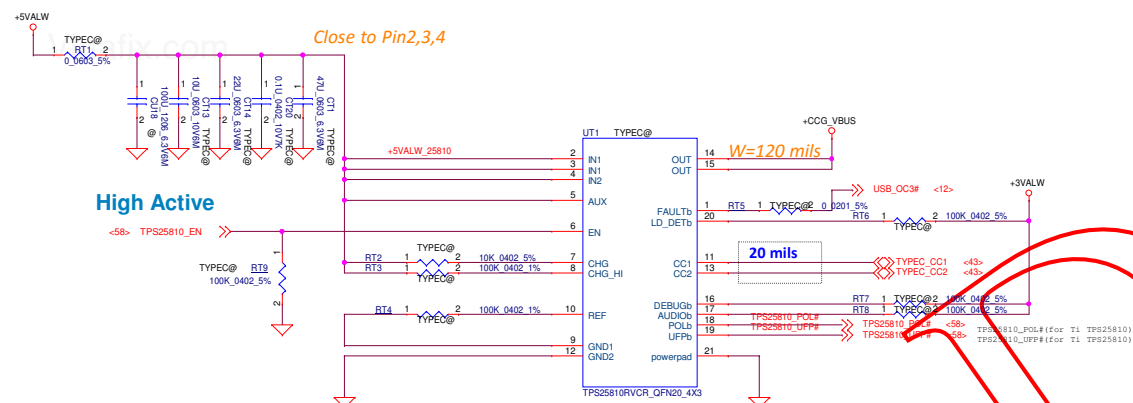
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				LA-G717P	
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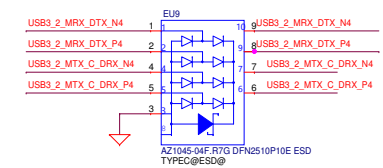
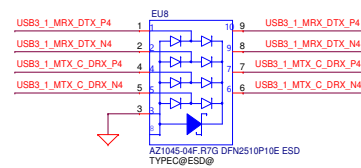
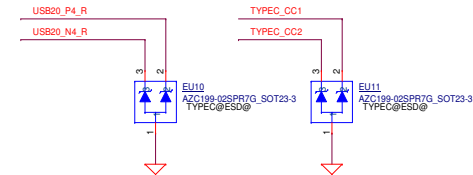
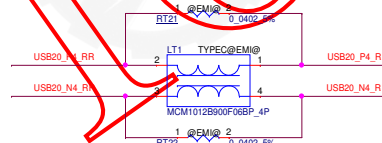
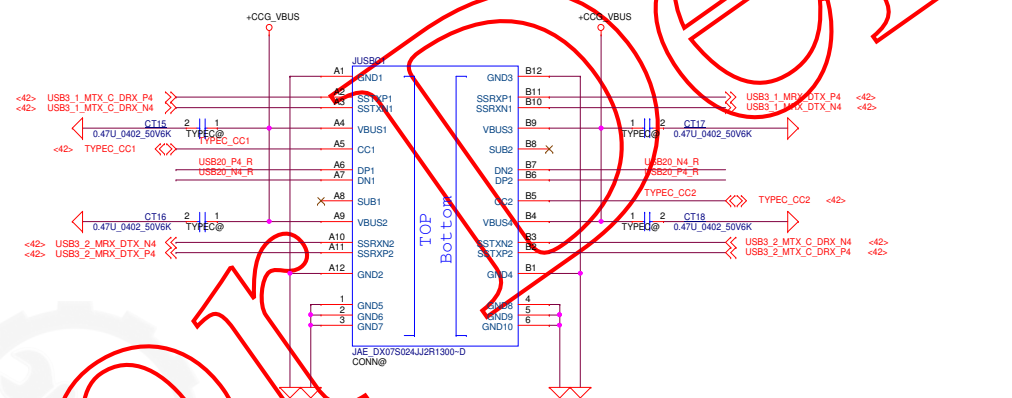
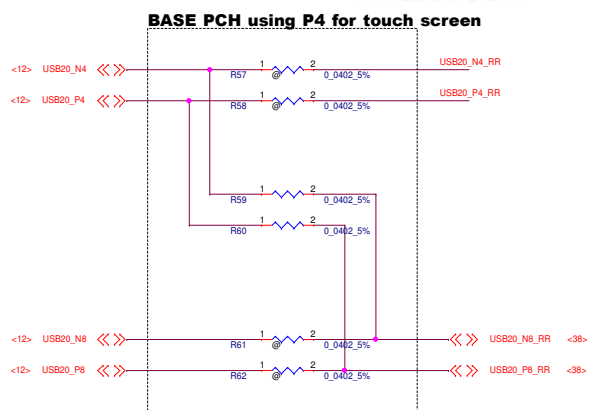


**5V@3A**

[illegible]

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Main Function: TYPE-C\_Power Path

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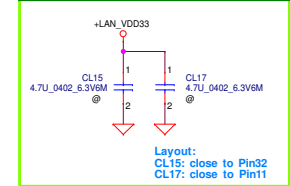
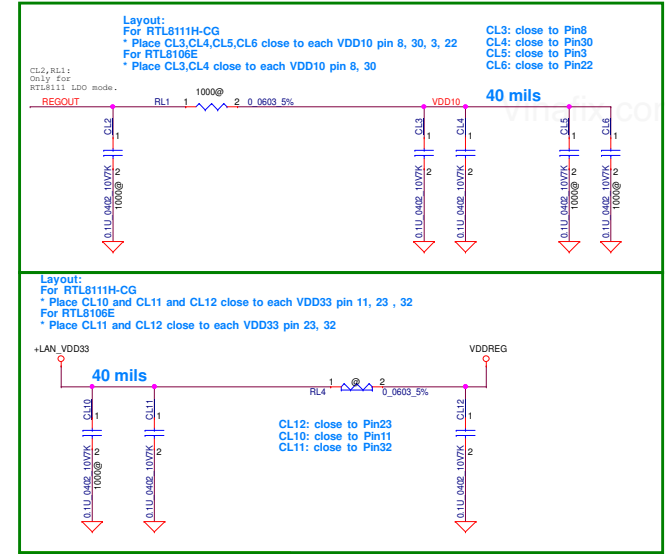
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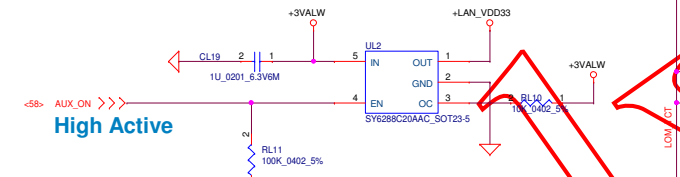
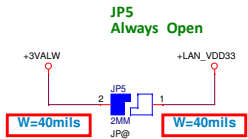
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Main Func = LAN

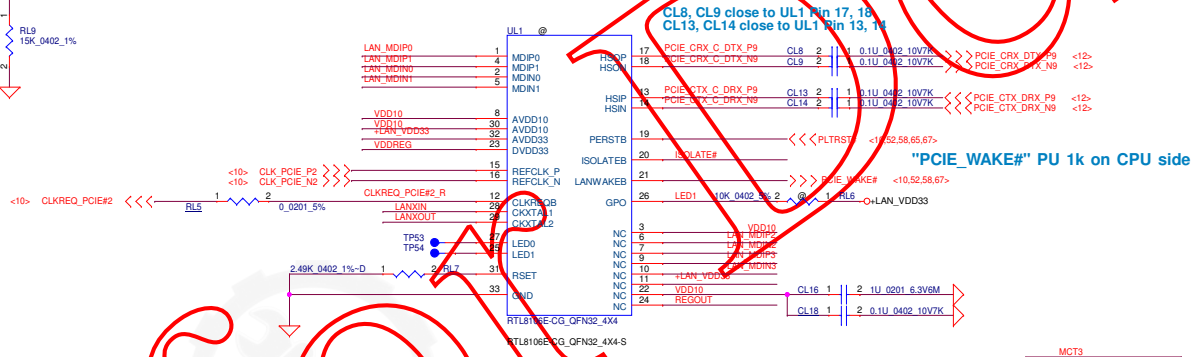
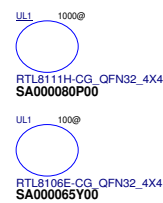
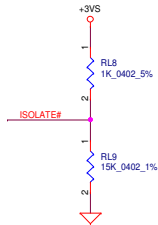


+LAN\_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

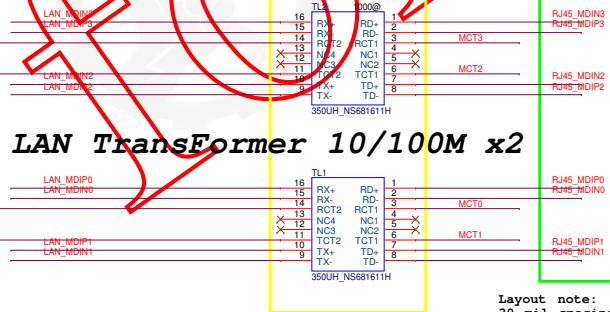


LAN CHIP 10/100/1000

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M



LAN TransForm 10/100M x2



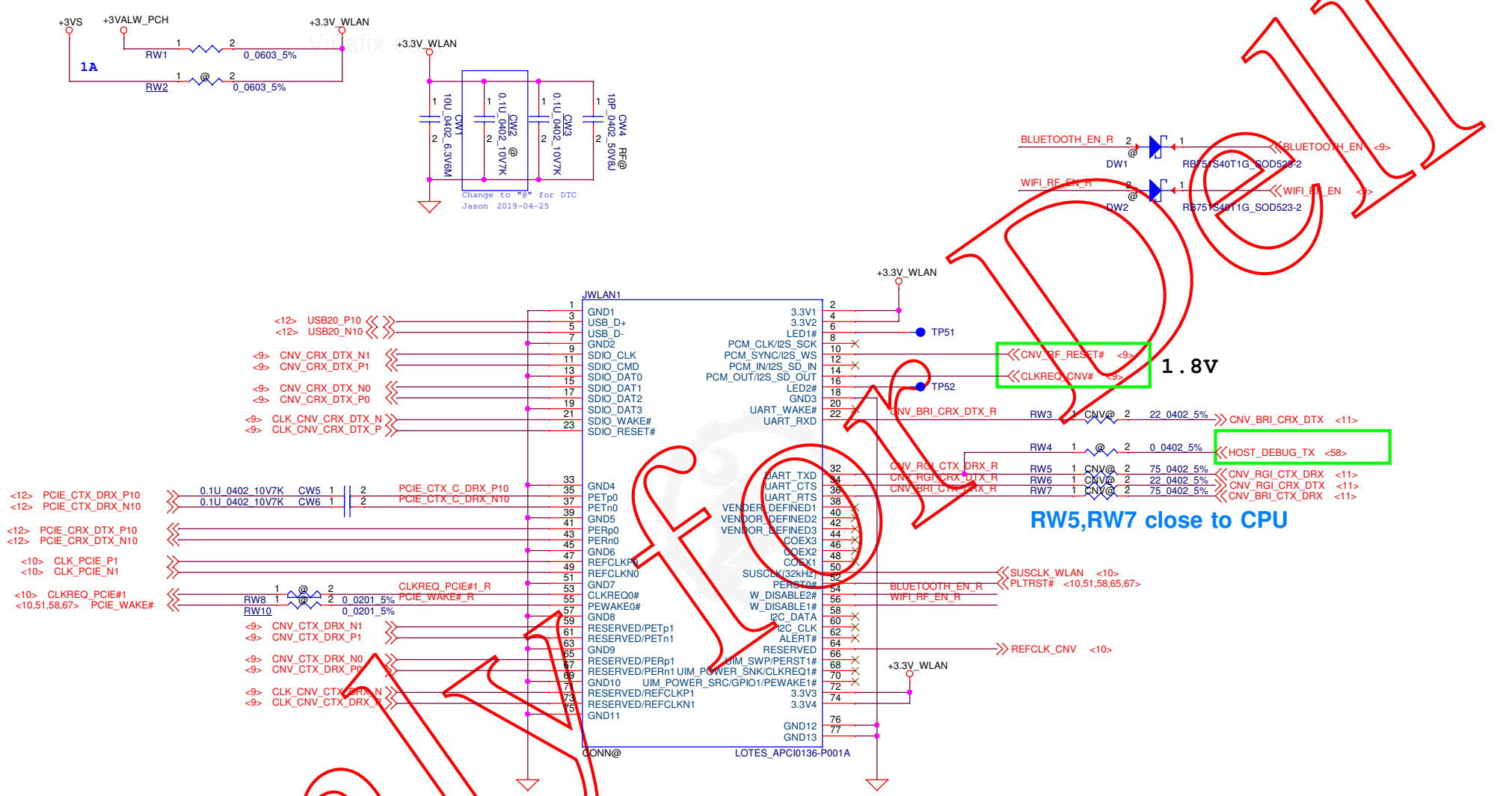
Layout note:  
30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF-0.4uF

	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O



Main Func = WLAN E Key CONN



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Main Function: WIGIG / WIDI

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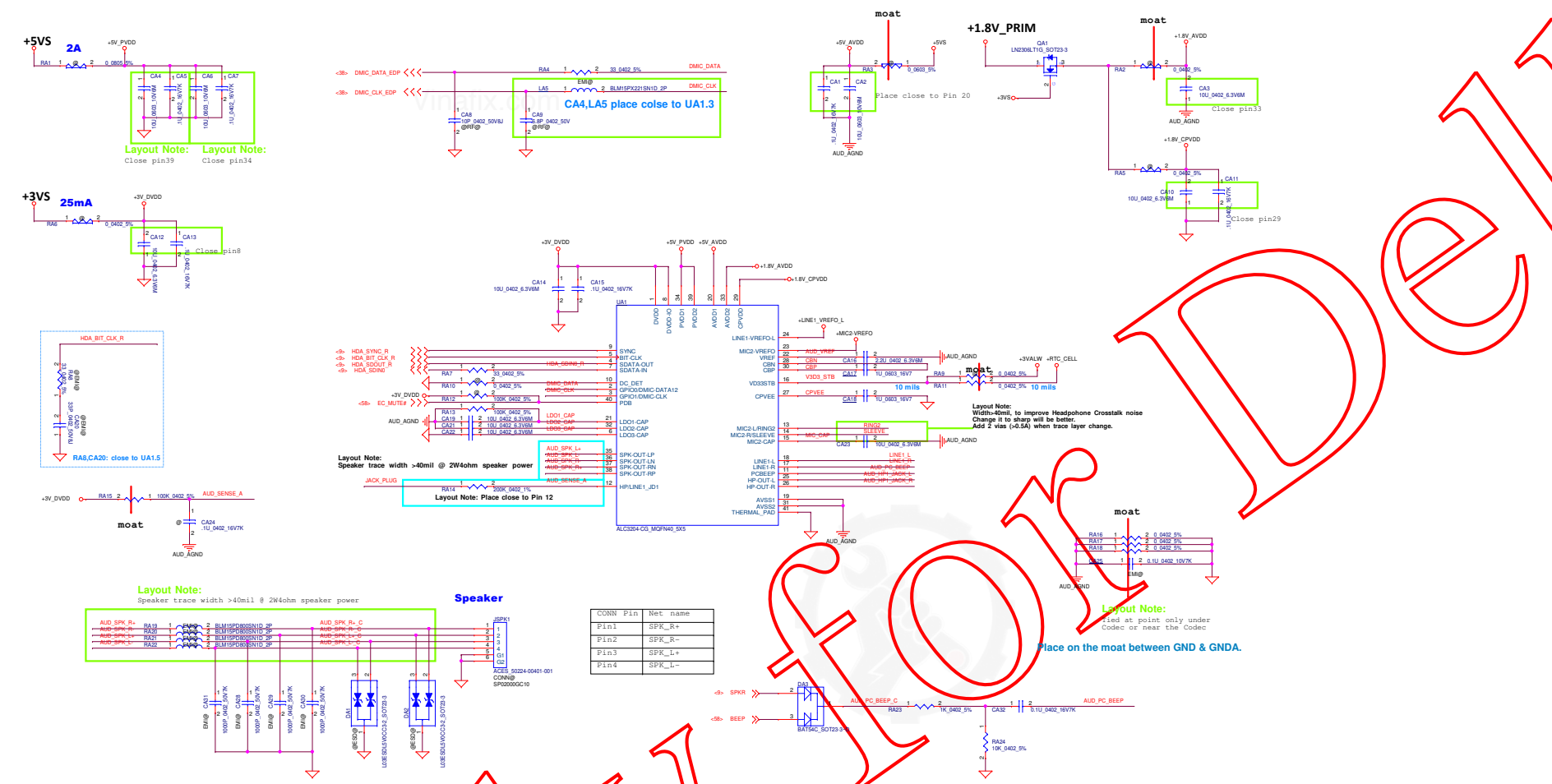
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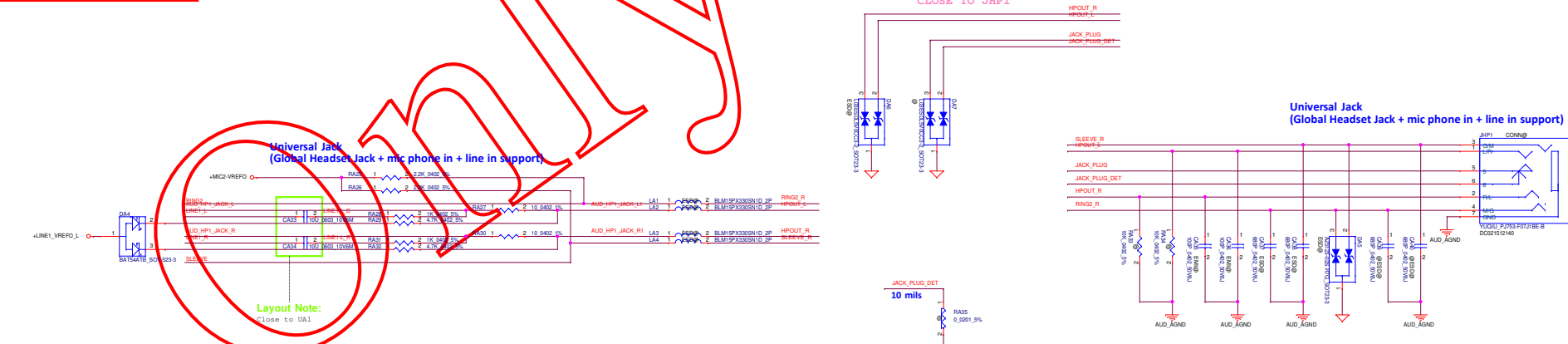
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Main Func = Audio EMI0, RF0, @EMI0, @ESD0, @RF0



Main Func = Audio Jack





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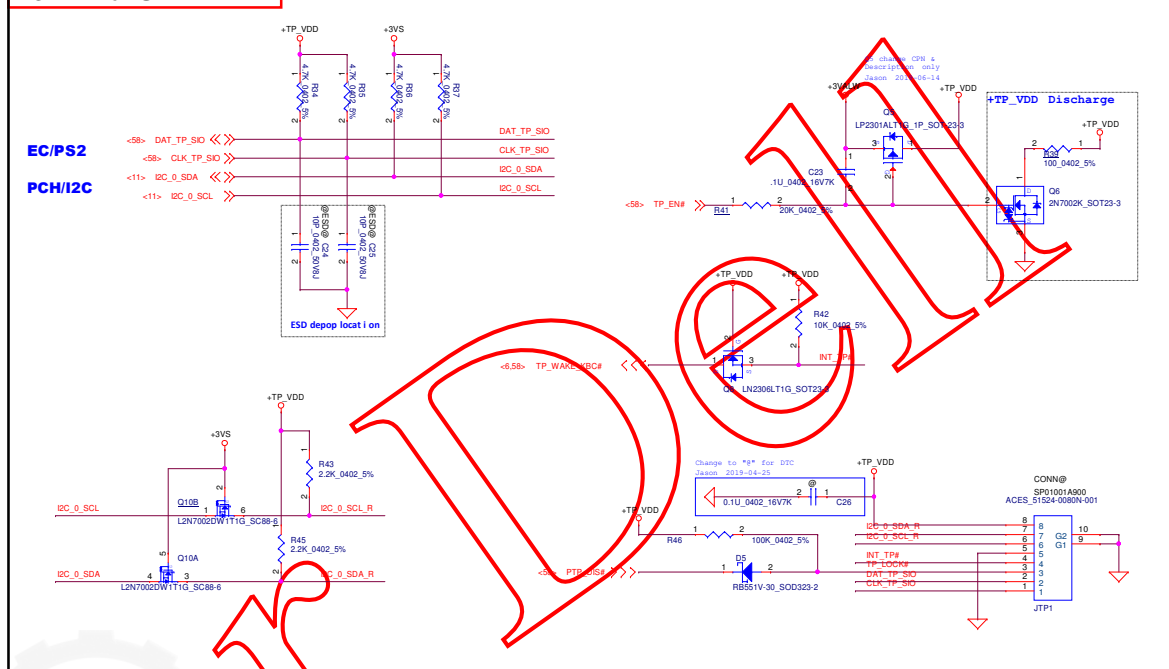
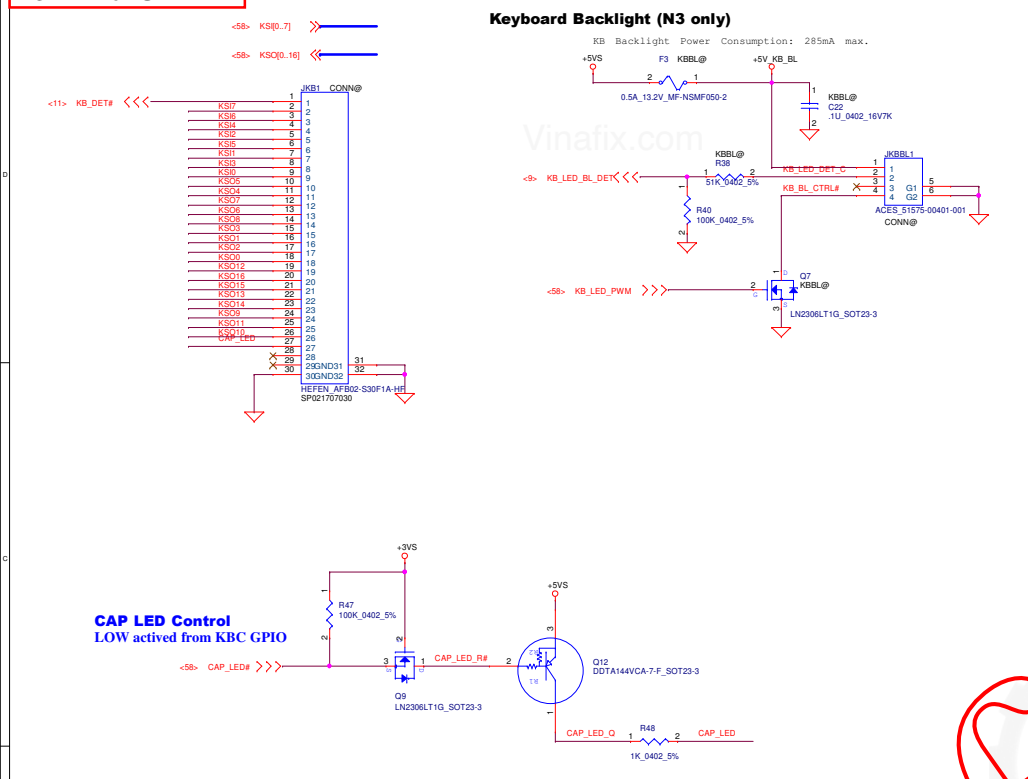
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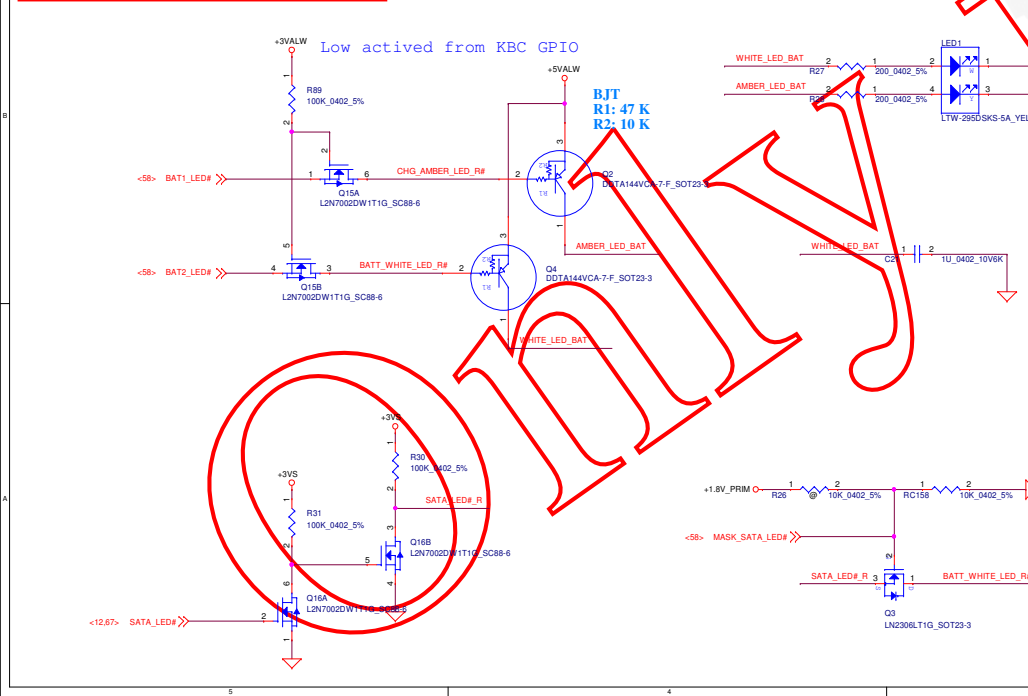
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3  
Main Func = TPAD



**Main Func = Battery LED**



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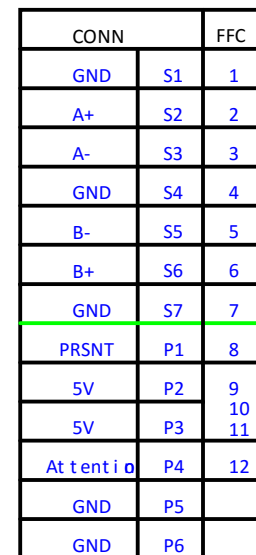
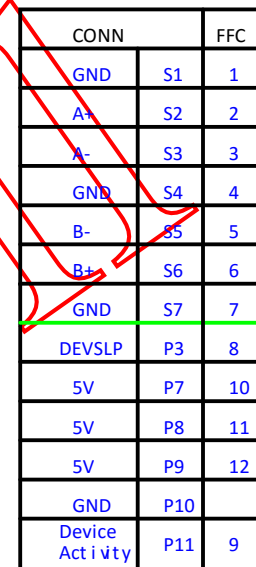
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**Main Func = ODD**



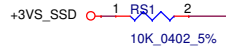
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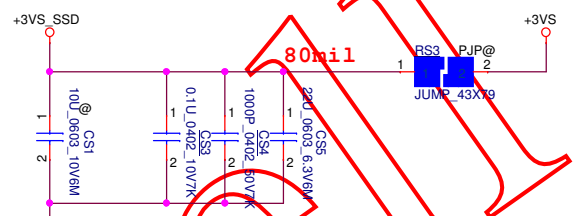
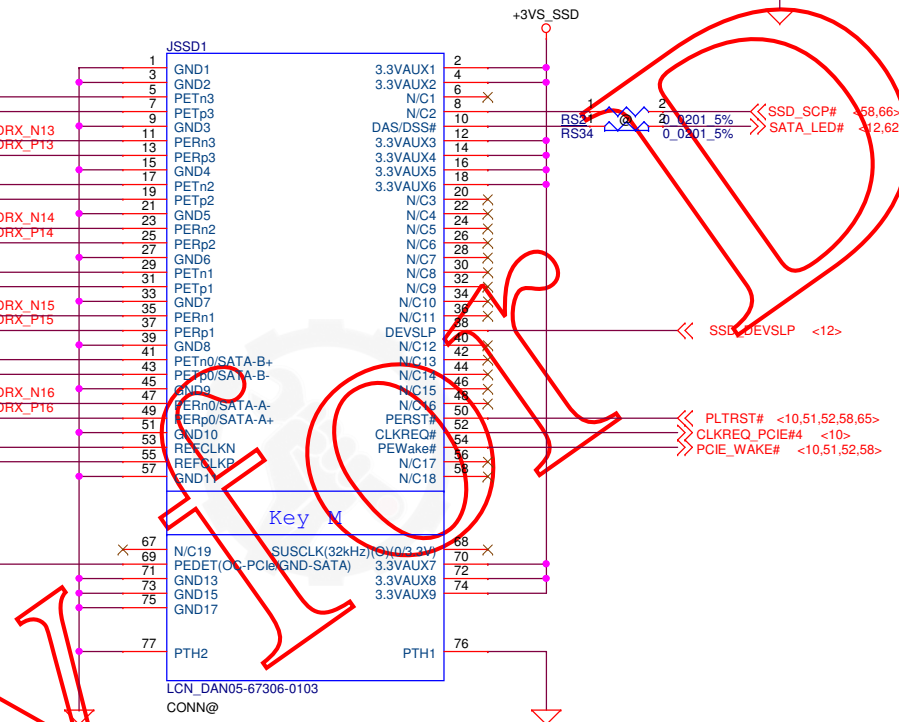
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NGFF Key M

- <12> PCIE\_CRX\_DTX\_N13
- <12> PCIE\_CRX\_DTX\_P13
- <12> PCIE\_CTX\_DRX\_N13
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PEDET	Module Type
0	SATA
1	PCIE





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Main Function:

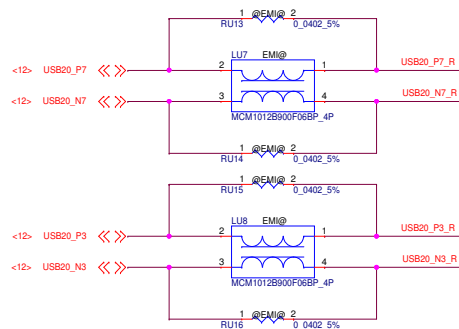
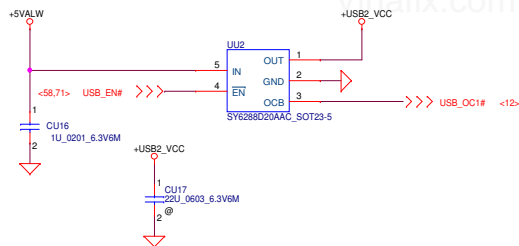
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Reserved

Only for Del

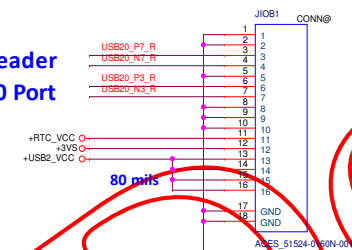
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## USB2.0/Card Reader connector

CardReader  
USB2.0 Port





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					LA-G717P	1.0
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				Size	Document Number	Rev
					LA-G717P	1.0
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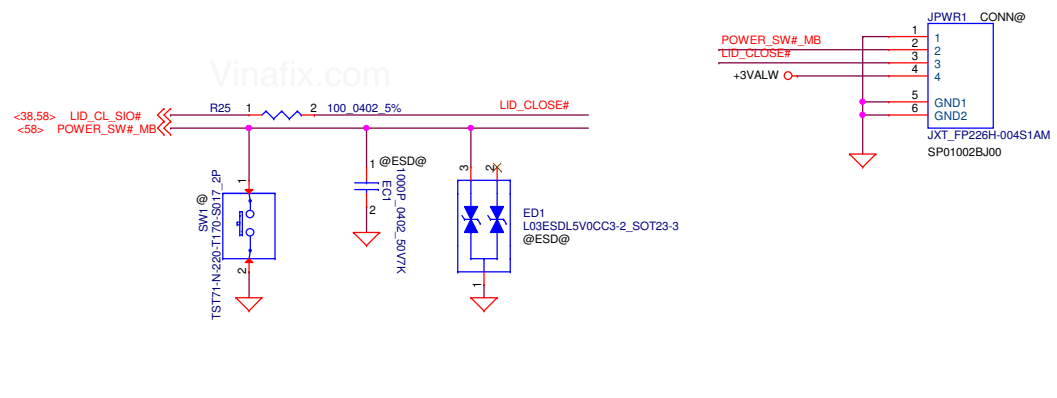
Reserved

Only for Del

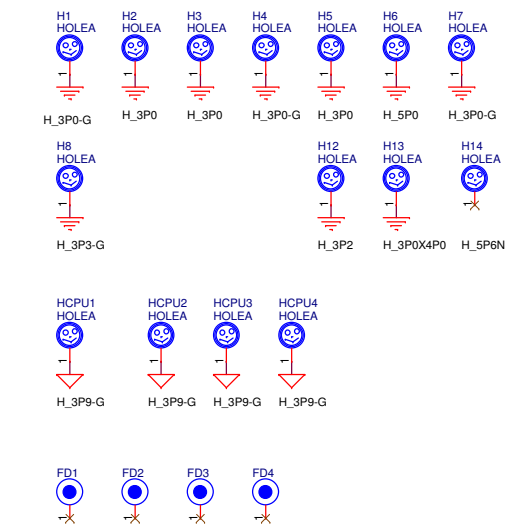
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				LA-G717P	
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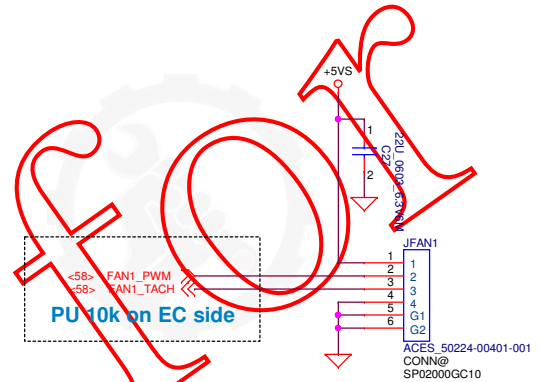
Main Func = Power BTN Low activated from KBC GPIO



Screw hole/FD



FAN

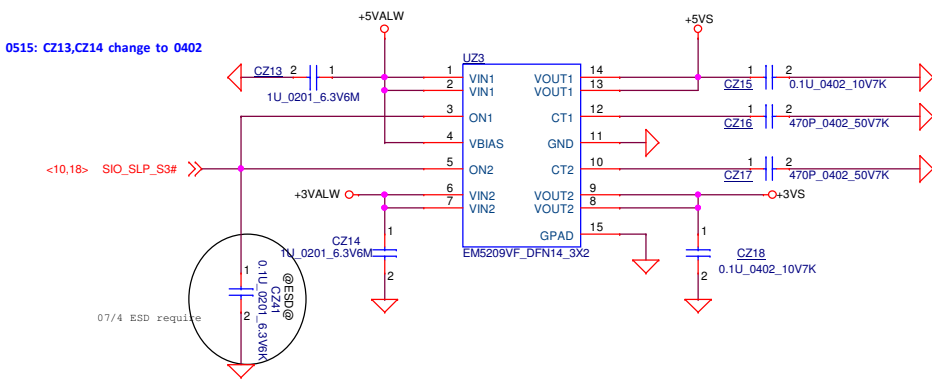


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				Size	Document Number
				LA-G717P	
Date: Wednesday, June 19, 2019		Sheet 77 of 100		Rev 1.0	



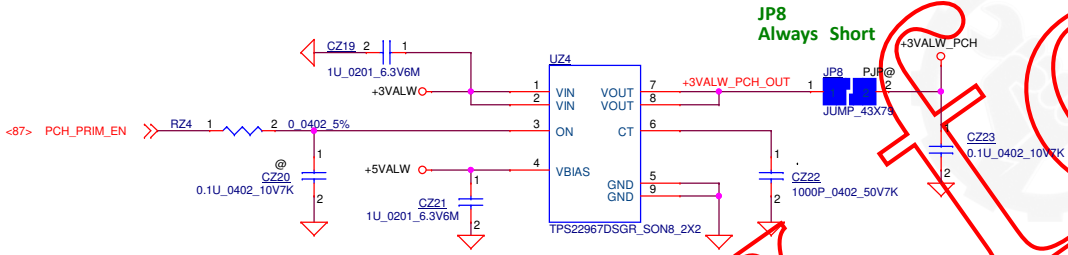
+5VS/+3VS for System

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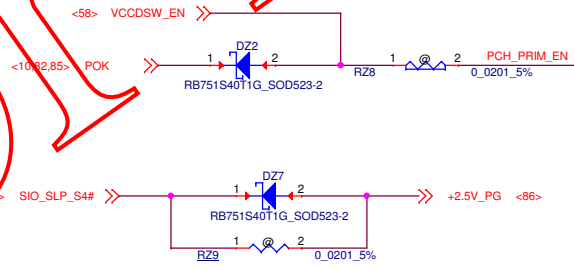
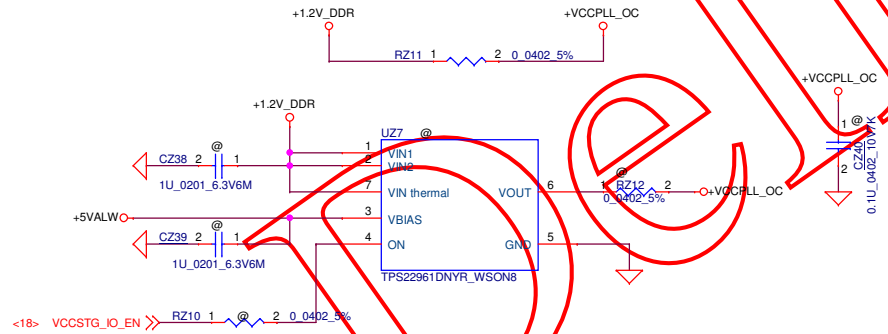


+3VALW\_PCH for System

JP8  
Always Short



+VCCPLL\_OC source

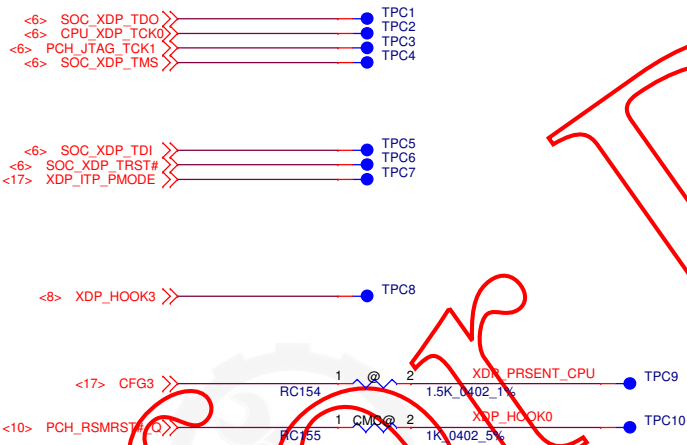
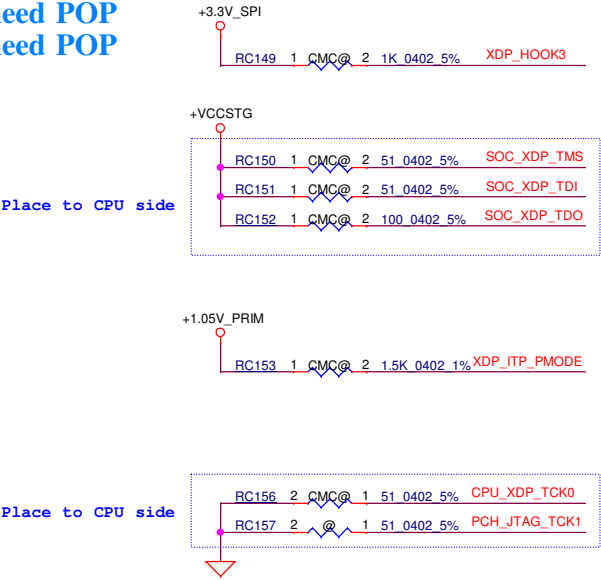


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PortConnector Less Routing Topology

Follow KBL DCI Link  
RC152 need POP  
RC156 need POP



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Main Func = Power Monitor

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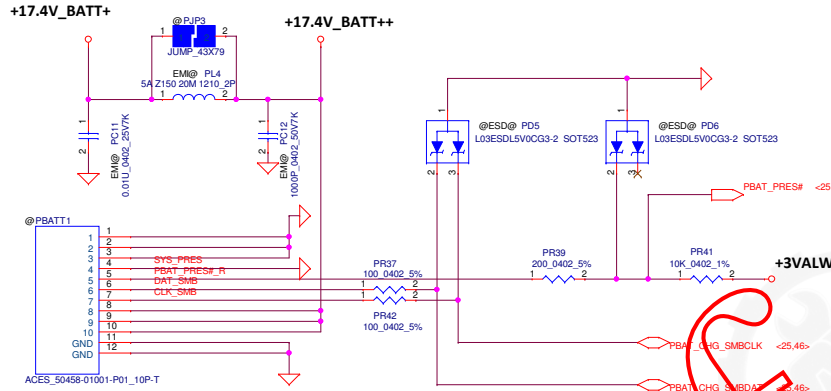
Main Func = BATT CONN

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Bat tery Bat Side

PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SYS\_PRES  
PIN5 BATT\_PRS  
PIN6 DAT\_SMB  
PIN7 CLK\_SMB  
PIN8 Bat t+  
PIN9 Bat t+  
PIN10 Bat t+  
SP021412220

ACES\_50458-01001-P01\_10P-T



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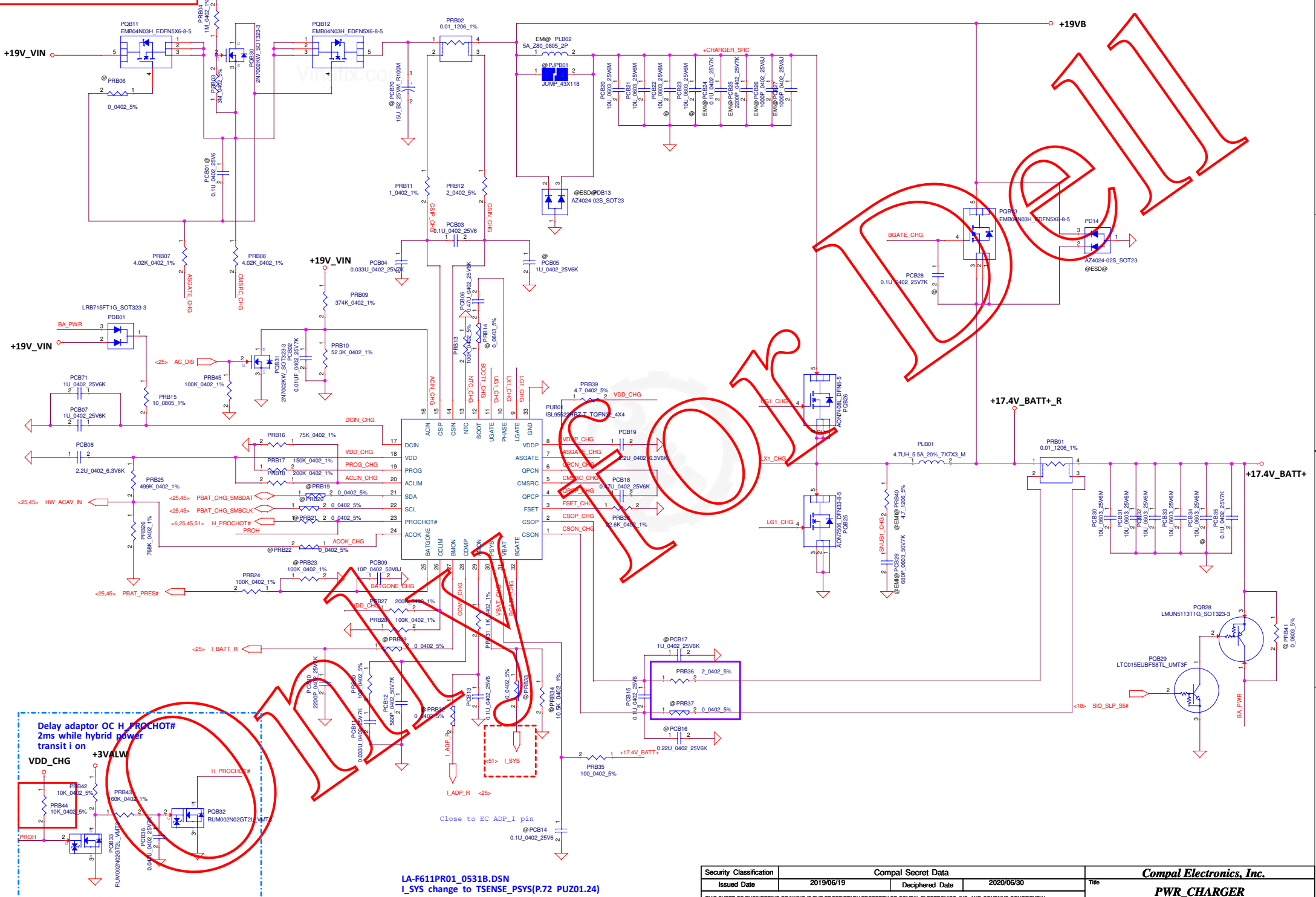
Compal Electronics, Inc.

PWR\_BATT\_CONN

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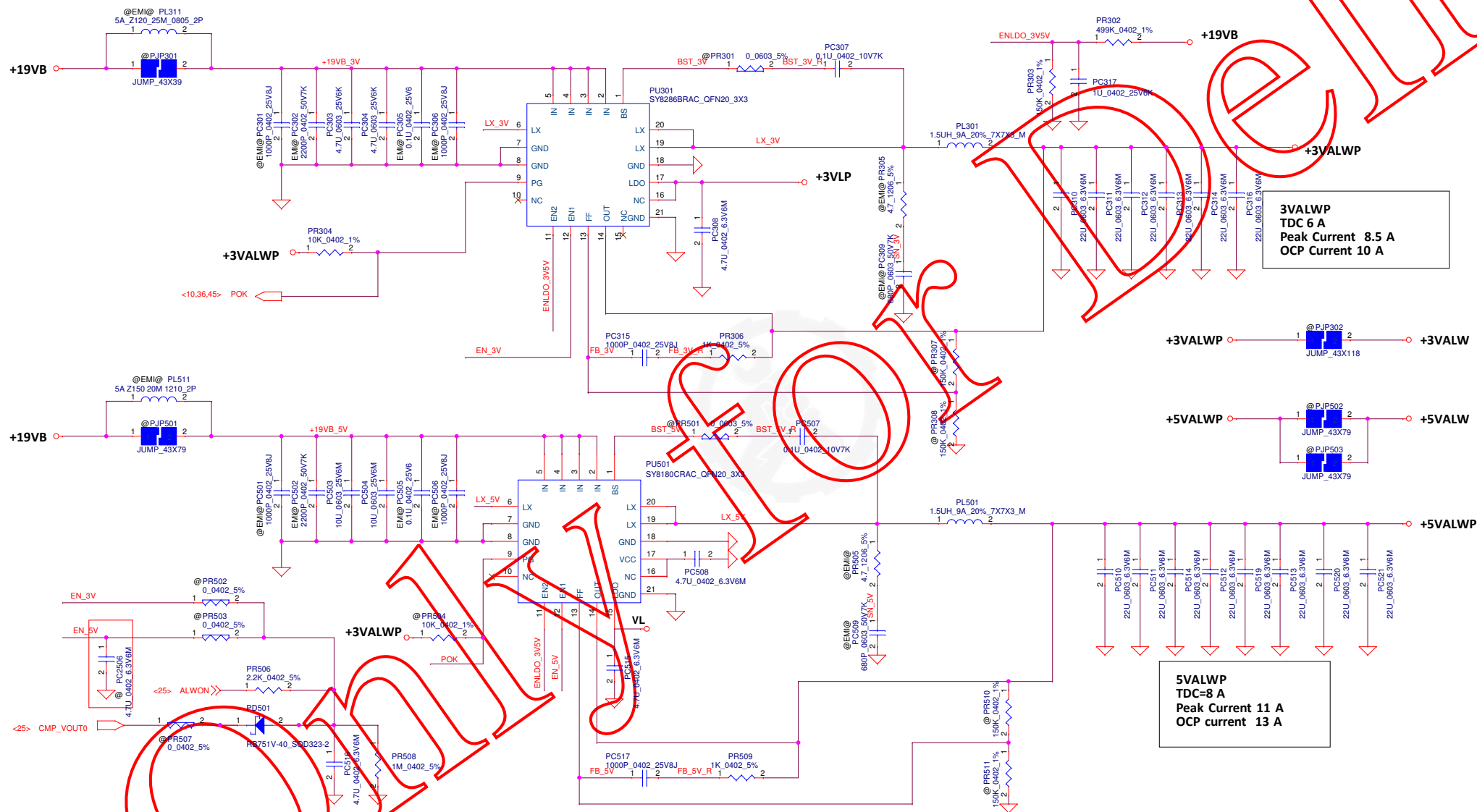
**Main Func = CHARGER**



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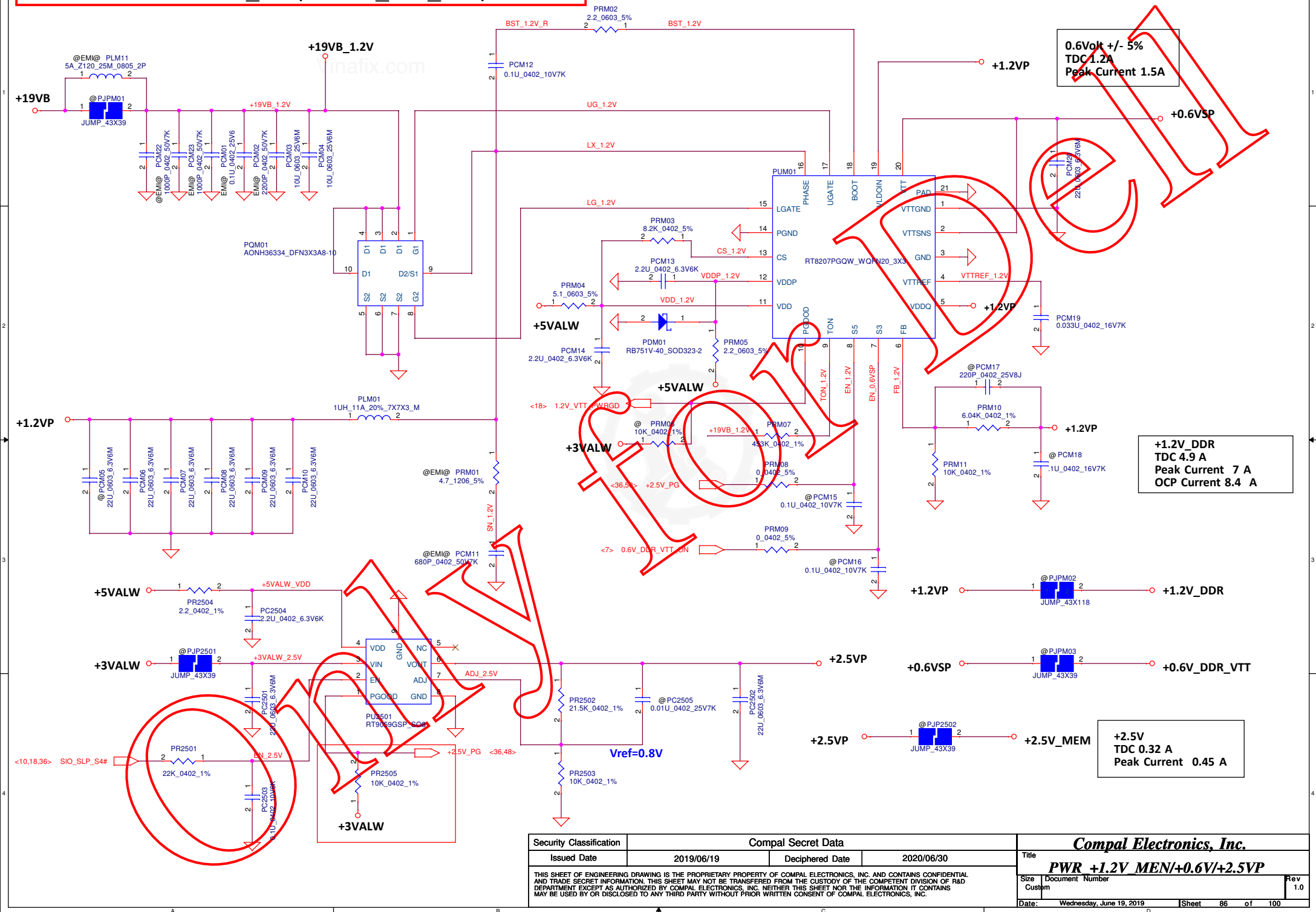
Main Func = 3.3VALWP/5VALWP



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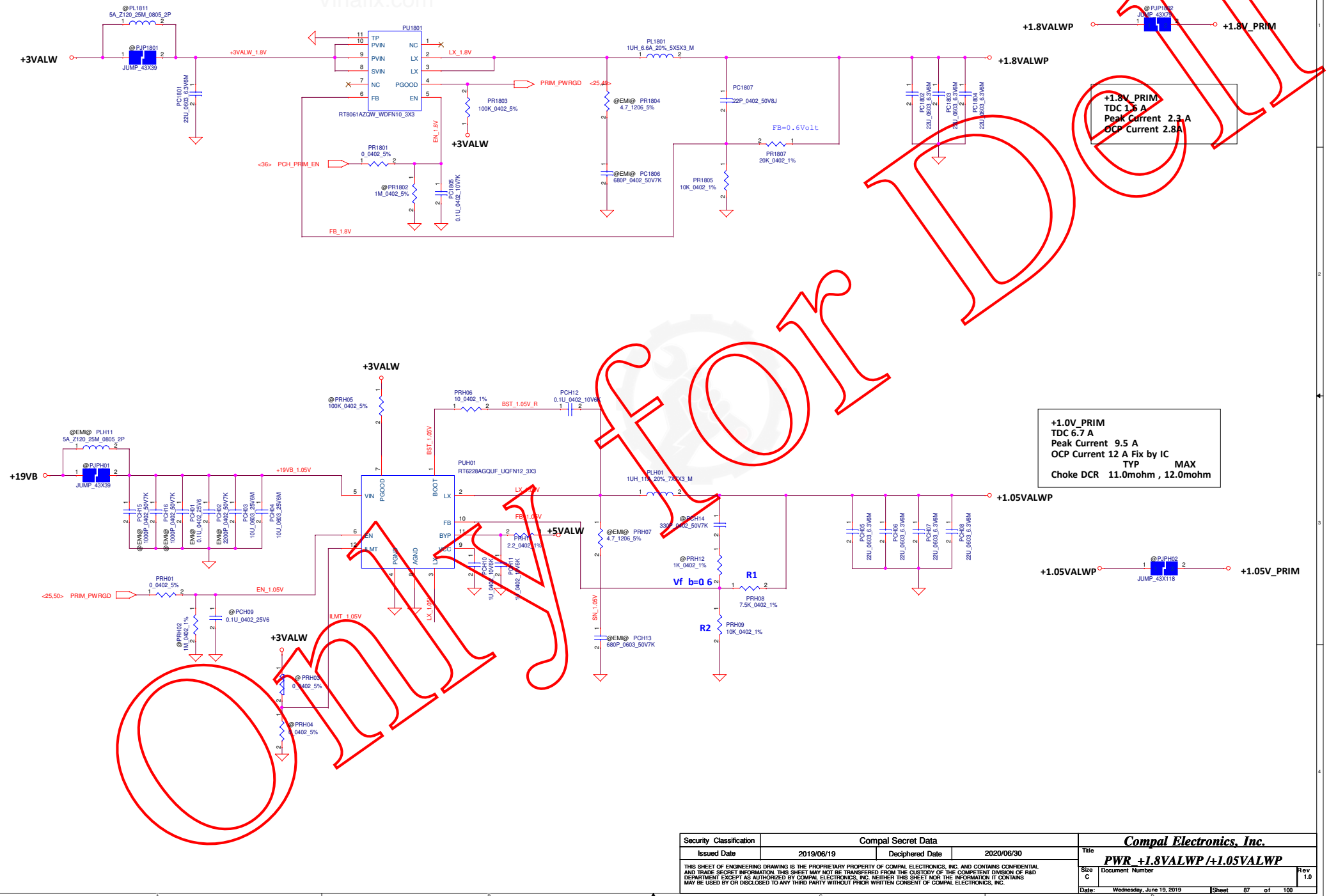


Main Func = +1.2V\_DDR/+0.6V\_DDR\_VTT/ +2.5VP





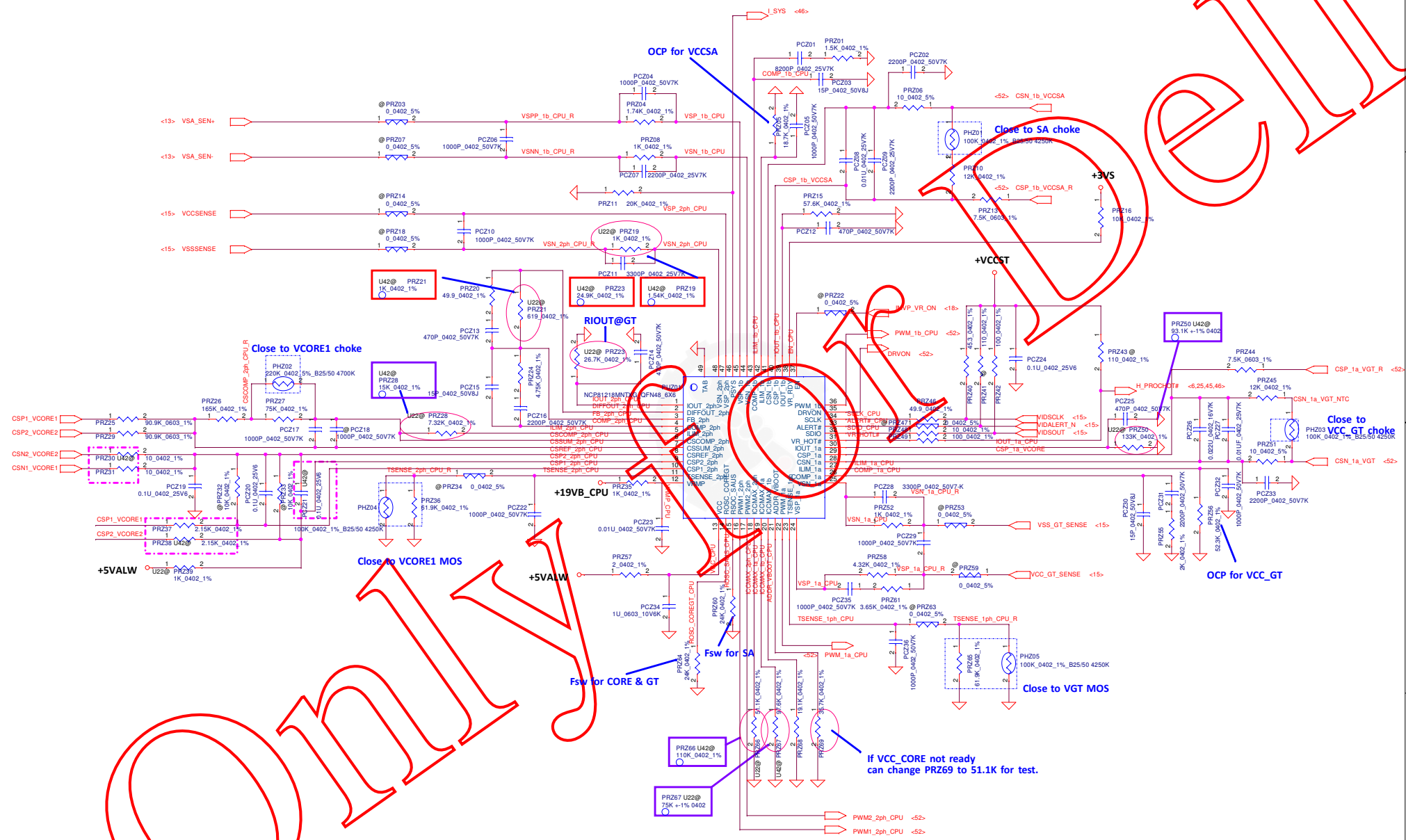
Main Func = +1.8VALWP / +1.05VALWP





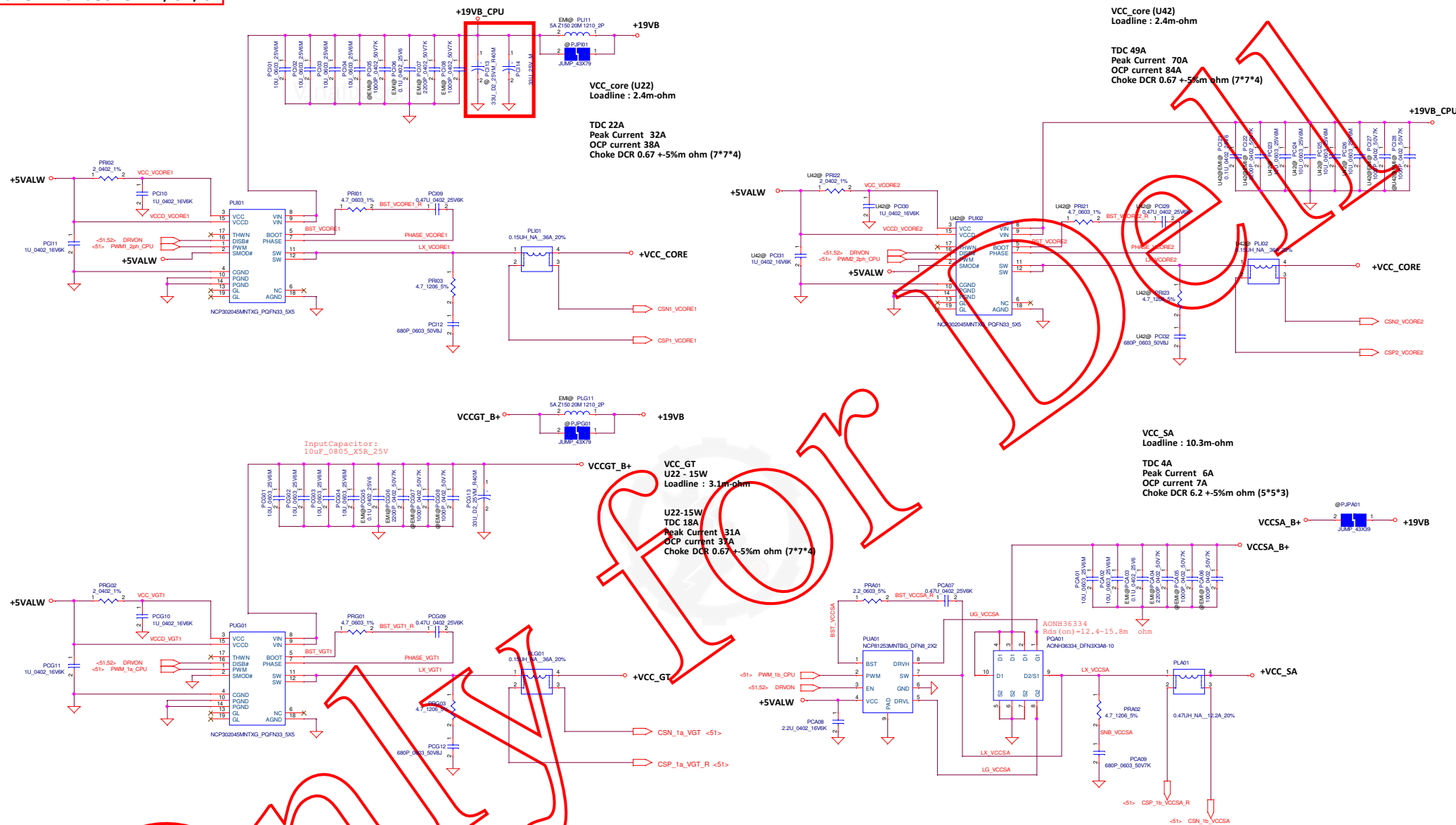
Main Func = CPU

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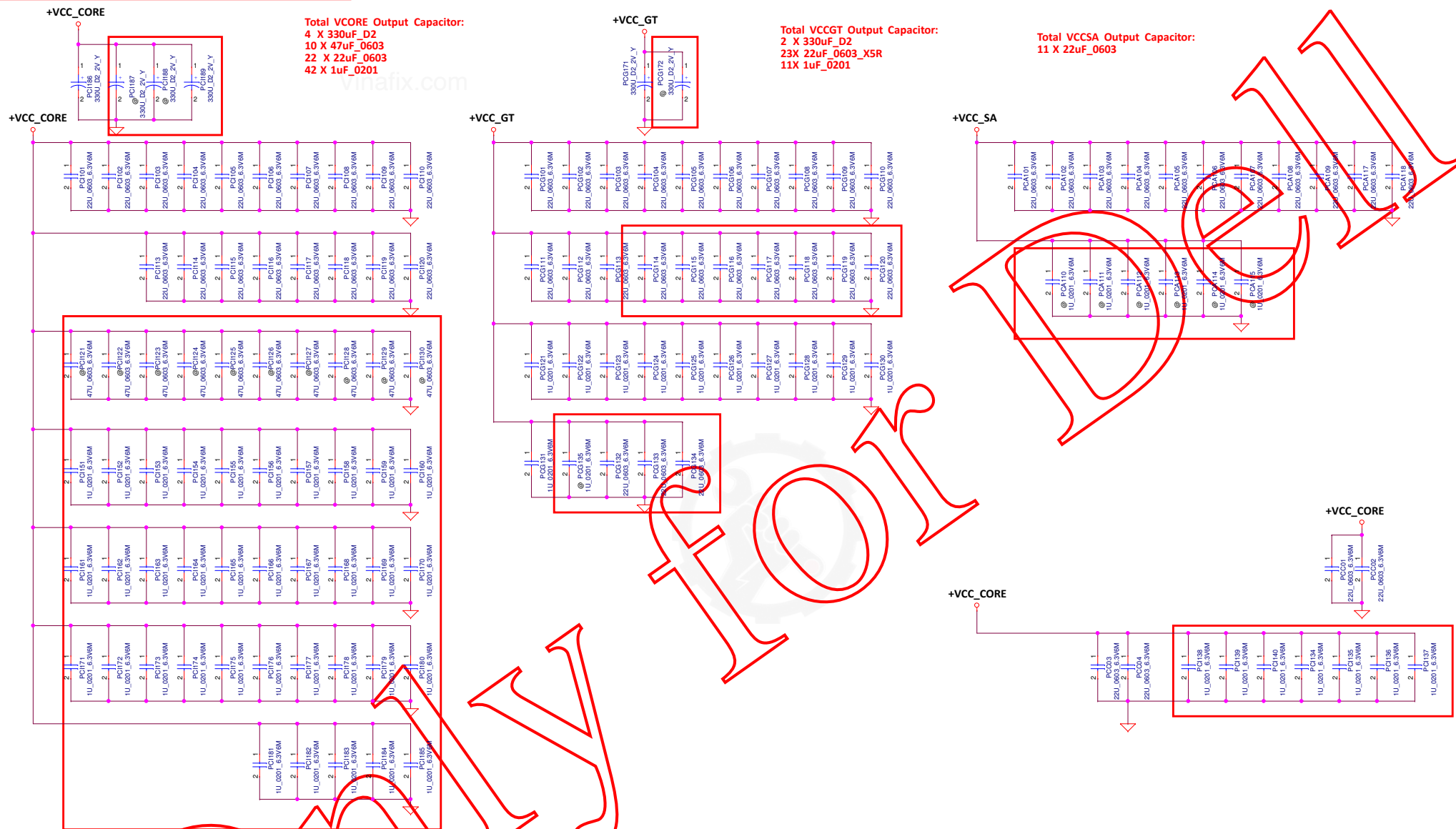
Main Func = CPUcore IA/GT/SA



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				PWR CPUcore IA/GT/SA	
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**Main Func = CPU/ VGA / SA MLCC**



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Version Change List ( P. I. R. List )

DVT1 EE change list

Design Change					
Item	Date	Page	Part reference	Change description	Reason
Based on 05/15					
1	2018/5/17	8		Add RC207, CPU_SPI_0_CS#1	For 2nd ROM
2	2018/5/17	14		CC52,CC48,CC51,CS change to 0402	meet purchase requirement
3	2018/5/17	29		CV73*CV78, CV100*CV109 change to 0402	meet purchase requirement
4	2018/5/20			Del C56,CU3,CU8; CU13,CU16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize
5	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch
6	2018/6/4	38		Connect UCL1,CC30 to R72, Add RC208,RC209	For 17" Touch
7	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize
8	2018/6/4	16		CL16 change to 0201	MLCC downsize
9	2018/6/13	56		CA16 change to 0402	MLCC downsize
10	2018/6/19	71		Swap D+/D- on JUSB1 Conn	For BITS377044
11	2018/6/19	38		Add LCD_CBI_DET# on Jedp pin14 and Connect to GPP_C10	For BITS378028
12	2018/7/4	65		add Rx10*14	co-lay ST TPM
13	2018/7/4			add CC75,C241,CC76,CC77,CC78,CC79	For ESD requirement
14	2018/7/6	65		add Rx15*RX19	co-lay China TPM



Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL			0.1 (X00)
2	P56	PWR	20160321	COMPAL			0.1 (X00)
3							
4							
5							
6							
7							
8							